SAE International

SURFACE VEHICLE RECOMMENDED PRACTICE

SAE J2602-2 NOV2012

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Superseding J2602-2 SEP2005

LIN Network for Vehicle Applications Conformance Test

RATIONALE

Usage of SAE J2602-2 over the past few years have uncovered some errors in the tests and typos in the documents. As new parts have been developed with additional functionality questions have been raised as to the preferred behavior of these devices. The release of the spec corrects these errors and answers the known questions that have arisen.

This update has removed references to the LIN 2.0 Conformance tests and has replaced them with tests in this document such that this document includes the entire required J2602-1 test suite.

FOREWORD

The objective of this document is to define a standard conformance test for SAE J2602-1 devices.

The goal of this document is to define a basic conformance test for SAE J2602-1 Master and Slave nodes that can be used to determine the suitability of devices for use. This is not a complete Qualification test. This does not replace the individual suppliers' IC and/or module qualification.

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TO PLACE A DOCUMENT ORDER: **Tel: 877-606-7323 (inside USA and Canada)**
Tel: +1 724-776-4970 (outside USA)
Fax: 724-776-0790
Email: CustomerService@sae.org
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http://www.sae.org/technical/standards/J2602/2_201211

1. SCOPE

This document covers the tests to be performed on all SAE J2602-1 defined Master and Slave nodes. Tests described in this document will ensure a minimum standard level of performance to which all compatible Electronic Control Unit (ECUs) and media shall be designed. This will assure full serial data communication among all connected devices regardless of supplier.

The goal of SAE J2602-2 is to improve the interoperability and interchangeability of LIN devices within a network by verifying the devices pass a minimum set of tests.

To allow for easy cross-reference, this document is arranged such that the conformance test for a given section in SAE J2602-1 is in the same section in SAE J2602-2.

This document is to be referenced by the particular vehicle Original Equipment Manufacturer (OEM) component technical specification that describes any given ECU in which the LIN data link controller and physical layer interface is located. Primarily, the performance of the physical layer is specified in this document. ECU environmental and other requirements, when provided in the component technical specification, shall supersede the requirements of this document.

The intended audience includes, but is not limited to, ECU suppliers, LIN controller suppliers, LIN transceiver suppliers, component release engineers and vehicle system engineers.

1.1 Mission/Theme

This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor and/or dedicated logic devices (ASICs) which use the network.

1.2 Overview

LIN is a single wire, low cost, Class A communication protocol. LIN is a master-slave protocol, and utilizes the basic functionality of most Universal Asynchronous Receiver Transmitter (UART) or Serial Communication Interface (SCI) devices as the protocol controllers in both Master and Slave devices. To meet the target of "Lower cost than either an OEM proprietary communications link or Controller Area Network (CAN) link" for low speed data transfer requirements, a single wire transmission media based on the ISO 9141 specification was chosen. The protocol is implemented around a UART/SCI capability set, because the silicon footprint is small (lower cost). Many small microprocessors are equipped with either a UART or SCI interface (lower cost), and the software interface to these devices is relatively simple to implement (lower software cost). Finally, the relatively simplistic nature of the protocol controller (UART/SCI) and the nature of state-based operation, enable the creation of Application Specific Integrated Circuits (ASICs) to perform as input sensor gathering and actuator output controlling devices, in the vein of Mechatronics.

All message traffic on the bus is initiated by the Master device. Slave devices receive commands and respond to requests from the Master. Since the Master initiates all bus traffic, it follows that the Slaves cannot communicate unless requested by the Master. However, Slave devices can generate a bus wakeup, if their inherent functionality requires this feature.

The "LIN Consortium" developed the set of LIN specifications. The Consortium is a group of automotive OEMs, semiconductor manufacturers, and communication software and tool developers. The LIN specification set is "released" by the LIN Steering Committee, a closed subset of the members. Associate Consortium members contribute to the formation of the specifications through participation in LIN Work Groups; however, the direction of the Work Groups and the final released content of the specifications is the responsibility of the LIN Steering Committee.

The LIN Conformance Test Specification contains tests for the Physical Layer, Data Link Layer, Node Configuration and Network Management, and EMC.

1.3 Relationship to the LIN Conformance Test Specification

This document includes all required tests for a J2602-1 node. This document no longer references the LIN Conformance Test Specification Package, version 1.0 dated August 1, 2004.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1213-1 Glossary of Vehicle Networks for Multiplexing and Data Communications

SAE J1930 Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviations, and Acronyms—Equivalent to ISO/TR 15031-2

SAE J2602-1 LIN Network for Vehicle Applications

SAE J2602-3 File Structures for a Node Capability File (NCF)

2.1.2 ISO Documents

Available from American National Standards Institute, 25 West 43rd Street, New York, NY 10036-8002, Tel: 212-642-4900, www.ansi.org.

ISO 9141 Road vehicles - Diagnostic systems - Requirements for interchange of digital information

2.1.3 Supplier Publications

See Appendix A for list of supplier documents/devices.

2.1.4 Other Publications

LIN Specification Package version 2.0 dated September 23, 2003 available at www.lin-subbus.org

ES-XW7T-1A278-AC - Ford Component and Subsystem Electromagnetic Compatibility Worldwide Requirements and Test Procedures available at www.fordemc.com. This document shall be referred to as the Ford EMC Spec.

3. DEFINITION OF TERMS

3.1 Glossary

3.1.1 Aging Factor of the Clock

This is provided by the supplier of the clock device (crystal, ceramic resonator, etc.) and is the portion of the maximum total clock tolerance over the device lifetime due to aging (time).

4. ACRONYMS, ABBREVIATIONS, AND SYMBOLS

API	Application Program Interface
ASIC	Application Specific Integrated Circuit
CAN	Controller Area Network
CTS	Component Technical Specification
DLC	Diagnostic Link Connector
DNN	Device Node Number
DUT	Device Under Test
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ISO	International Organization for Standardization
Kbits/s	Thousands of data bits per s
LDF	LIN Description File
LIN	Local Interconnect Network
LSB	Least Significant Byte
Lsb	Least significant bit
MSB	Most Significant Byte
Msb	Most significant bit
NAD	Node Address for Diagnostics
NCF	Node Capability File
OEM	Original Equipment Manufacturer
RE	Radiated Emissions
RI	Radiated Immunity
SCI	Serial Communication Interface
UART	Universal Asynchronous Receiver/Transmitter

5. LIN SYSTEM REQUIREMENTS

General Test Assumptions

1 All slave devices shall have at least one request message to which they respond.

2 The Cload and Rload values specified shall include the characteristics of the test tool, so that this is the entire load external to the DUT.

3 All slave devices are assumed to contain 220 pF nominal capacitance and 30 K nominal resistance.

4 All Master devices are assumed to contain 680 pF nominal capacitance and 1K nominal resistance.

5 The power supply voltage shall be 12 V unless otherwise specified.

6 The ambient temperature shall be between 20 and 28 °C (68 and 82.4 °F).

7 The length of each wire segment shall be between 0.5 and 2 m in length unless otherwise specified.

8 Each wire segment shall consist of 20 or 22 gauge copper wire.

9 The value of all external load resistors shall be within 0.1% of the specified resistance value.

10 The value of all external load capacitors shall be within 1.0% of the specified capacitance value.

5.1 LIN Specification Package

This section is informative in nature and does not require any tests.

5.2 J2602-1 Serial Data Link Characteristics

This section is informative in nature and does not require any tests.

5.3 Detection of Errors by Master (reference 4.1, LIN 2.0 Protocol Specification)

This test verifies that the Master DUT stops transmitting the header when the Synch symbol is not $55 or when there is a framing error in the Synch symbol (STOP bit = 0).

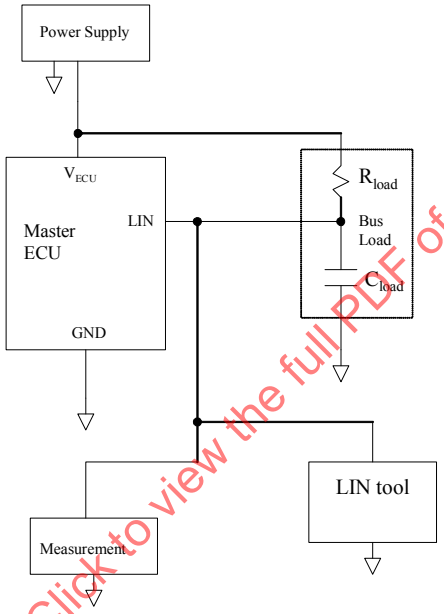

FIGURE 1 - DETECTION OF ERRORS BY MASTER TEST SETUP

TABLE 1A - DETECTION OF ERRORS BY MASTER TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 5.3.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V 30 kΩ, 220 pF
Test Steps	See Table 1B	
Response	See Table 1B	
Reference	SAE J2602-1, 5.3	

TABLE 1B - DETECTION OF ERRORS BY MASTER TEST PLAN

# Test	Test Steps	Response
5.3.1	1. DUT sends out any message. 2. Test tool sends out a $F0 data byte when a Start bit is detected after the break symbol	The DUT must not transmit the ID. The next thing transmitted by the DUT must be a Break/Sync symbol.
5.3.2	1. DUT sends out any message. 2. Test tool corrupts the stop bit of the Sync Byte.	The DUT must not transmit the ID. The next thing transmitted by the DUT must be a Break/Sync symbol.

5.4 Frame Processing by Slave Tasks (reference 4.2.2, LIN 2.0 Protocol Specification)

5.4.1 Slave Node Error Behavior

The purposes of this test are to:

1. Verify that the slave DUT stops transmission when an error occurs during transmission and sets the appropriate error code in the J2602-1 Status Byte.

2. Verify that the slave DUT recognizes an error in a received message and sets the appropriate error code in the J2602-1 Status Byte.

3. Verify that the slave DUT does not transmit when the Synch byte is anything other than $55 and sets the appropriate error code in the J2602-1 Status Byte.

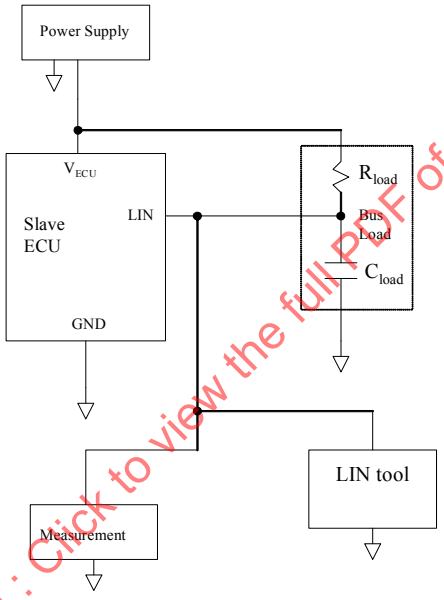

FIGURE 2 - SLAVE NODE ERROR BEHAVIOR TEST SETUP

TABLE 2A - SLAVE NODE ERROR BEHAVIOR TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.4.1.x (5 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	See Table 2B	
Response	See Table 2B	
Reference	SAE J2602-1, 5.4	

TABLE 2B - SLAVE NODE ERROR BEHAVIOR TEST PLAN

# Test	Test Steps	Response
5.4.1.1	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Targeted Reset to the DUT 3. Send a $3D Response with the ID Parity bits corrupted, i.e., Protected ID of (0011 1101) 4. Send a slave specific request message ID for DUT without error.	After step 3 the DUT must not send any data. After step 4 the Status Byte returned by the DUT must be (111x xxxx).
5.4.1.2	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a slave specific command message ID and Data for the DUT and corrupt the Stop bit (transmit a dominant) of the last data byte in the frame. 3. Send a slave specific request message ID for DUT without error.	After step 3 the Status Byte returned by the DUT must be (110x xxxx).
5.4.1.3	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Targeted Reset with a corrupted checksum to the DUT 3. Send a slave specific request message ID for DUT without error.	After step 3 the Status Byte returned by the DUT must be (101x xxxx).
5.4.1.4	1. x = 0 2. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 3. Send a $3C Targeted Reset to the DUT 4. Send a $3D Response with sync byte = x. 5. Send a slave specific request message ID for DUT without error. 6. x = x + 1 7. If x <= 255 goto 2, else END.	After step 4 the DUT must only transmit if the sync byte transmitted was $55. After step 5 the Status Byte returned by the DUT must be (100x xxxx) if the device has a fixed clock. Alternatively, if the device is performing autobauding and the SYNC byte was not $55, the Status Byte is ignored but a valid response shall be sent by the DUT..
5.4.1.5	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Targeted Reset to the DUT 3. Send a $3D Response and corrupt bit 6 (send a dominant) of the NAD byte sent by the DUT. 4. Send a slave specific request message ID for DUT without error.	After step 3 the DUT must not transmit another byte after the NAD. After step 4 the Status Byte returned by the DUT must be (100x xxxx).

# Test	Test Steps	Response
5.4.1.6	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Targeted Reset to the DUT 3. Send a $3D Response with the ID Parity bits corrupted, i.e. Protected ID of (0011 1101) 4. Send a $3C Targeted Reset with a corrupted checksum to the DUT 5. Send a $3D Response and corrupt bit 6 (send a dominant) of the NAD byte sent by the DUT. 6. Send a slave specific request message ID for DUT without error. 7. Send a slave specific request message ID for DUT without error. 8. Send a slave specific request message ID for DUT without error. 9. Send a slave specific request message ID for DUT without error. 10. Send a slave specific request message ID for DUT without error.	After step 3 the DUT should not send any data. After step 6 the Status Byte returned by the DUT should be (111x xxxx). After step 7 the Status Byte returned by the DUT should be (101x xxxx). After step 8 the Status Byte returned by the DUT should be (100x xxxx). After step 9 the Status Byte returned by the DUT should be (001x xxxx). After step 10 the Status Byte returned by the DUT should be (000x xxxx).

5.4.2 Slave Task in a Master Node Error Behavior

This test verifies that the Master DUT stops transmitting when there is an error in the Protected Identifier, a framing error in any data byte, or a data bit is corrupted.

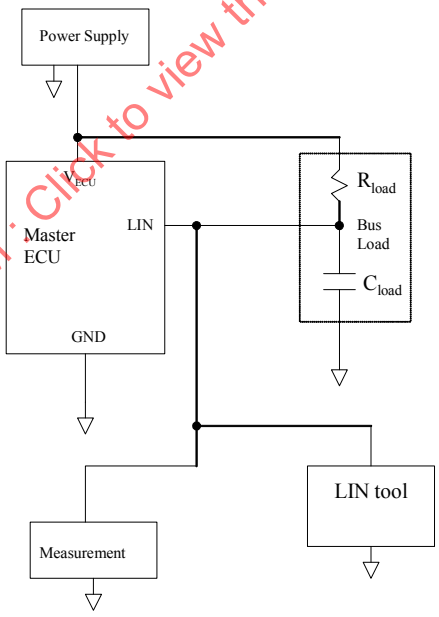

FIGURE 3 - SLAVE TASK IN A MASTER NODE ERROR BEHAVIOR TEST SETUP

TABLE 3A - SLAVE TASK IN A MASTER NODE ERROR BEHAVIOR TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 5.4.2.x (3 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V 30 kΩ, 220 pF
Test Steps	See Table 3B	
Response	See Table 3B	
Reference	J2602-1 Section 5.4	

TABLE 3B - SLAVE TASK IN A MASTER NODE ERROR BEHAVIOR TEST PLAN

# Test	Test Steps	Response
5.4.2.1	Corrupt the parity of the ID byte of any Command Message initiated by the DUT.	The DUT must not transmit any other bytes of this message. The next thing transmitted by the DUT must be a Break/Sync symbol.
5.4.2.2	Corrupt the stop bit of any data byte of any Command Message initiated by the DUT.	The DUT must not transmit any other bytes of this message. The next thing transmitted by the DUT must be a Break/Sync symbol.
5.4.2.3	Corrupt any single data bit of any data byte of any Command Message initiated by the DUT.	The DUT must not transmit any other bytes of this message. The next thing transmitted by the DUT must be a Break/Sync symbol.

5.5 Master and Slave Message Transmission Time Tolerance (reference 2.2, LIN 2.0 Protocol Specification)

Use the following messages for the Test Frames called out in this section:

TABLE 4 - TEST FRAME ASSIGNMENTS

TST_Frame	Requirements for the Test Frame
TST_FRAME_1	Any frame sent by the master
TST_FRAME_2	Targeted Reset
TST_FRAME_3	Not Used
TST_FRAME_4	Device Specific Frame, reference NCF
TST_FRAME_5	Not Used
TST_FRAME_6	Slave Response Command Frame, Identifier = 0x3D
TST_FRAME_7	Not Used
TST_FRAME_8	Not Used
TST_FRAME_9	Command Frame Sleep Request, Identifier = 0x3C, NAD = 0x00

Use the following values for the variables in this section:

TABLE 5 - TEST VARIABLE TIMES

Parameter	Time
T_{SYNBRK_MIN}	1241 µs
T_{SYNBRK_MAX}	2580 µs
T_{SYNDEL_MIN}	95 µs
T_{SYNDEL_MAX}	1422 µs
$T_{HEADER\_NOMINAL}$	3264 µs
$T_{HEADER\_MAXIMUM}$	4606 µs
$T_{FRAME\_NOMINAL}$	11904 µs
$T_{FRAME\_MAXIMUM}$	$T_{HEADER\_MAXIMUM}$ + safety_factor * 90 * max clock tol.
40 bits	3840 µs
20 bits	1920 µs
19 bits	1824 µs
15 bits	1440 µs
13 bits	1248 µs
10 bits	960 µs
8 bits	768 µs
6 bits	576 µs
3 bits	288 µs
2 bits	192 µs

NOTE: Maximum delays include 13.2 us for transceiver propagation delay (includes transmit and receive delays).

5.5.1 Length of SYNCH BREAK LOW PHASE (DUT as Master)

This test verifies that the DUT as Master transmits the correct length of the SYNCH BREAK LOW PHASE T_{SYNBRK} as defined in the LIN specification.

TABLE 6 - LENGTH OF SYNCH BREAK LOW PHASE TEST PLAN

DUT node as	Master ECU With C = 680pF	
Parameter	V_{ECU} Test Frames	12V TST_FRAME_1
Test Steps	The DUT sends TST_FRAME_1.	
Response	$T_{SYNBRK} \geq T_{SYNBRK\_MIN}$	
Reference	SAE J2602-1, 5.5	

5.5.2 Variation of Length of SYNCH BREAK LOW PHASE (DUT as Slave)

This test verifies that the DUT as slave recognises an ID request with different lengths of SYNCH BREAK LOW PHASE T_{SYNBRK}.

TABLE 7A - VARIATION OF LENGTH OF SYNCH BREAK LOW PHASE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.5.2.x (3 cases)
Parameter	V_{ECU} Test Frames	12V TST_FRAME_2, TST_FRAME_6
Test Steps	See Table 7B	
Response	See Table 7B	
Reference	SAE J2602-1, 5.5	

TABLE 7B - VARIATION OF LENGTH OF SYNCH BREAK LOW PHASE TEST PLAN

# Test	Test Steps	Response
5.5.2.1	1. The Test Tool as master sends TST_FRAME_2 with the length of SYNCH BREAK LOW PHASE T_{SYNBRK} as defined below. $T_{SYNBRK} = T_{SYNBRK\_MIN}$ $T_{SYNDEL} = T_{SYNDEL\_MIN}$ $T_{H\_Interbyte} = 0$ ($T_{H\_Interbyte}$ is the interbyte space between sync field and identifier) 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.2.2	1. The Test Tool as master sends TST_FRAME_2 with the length of SYNCH BREAK LOW PHASE T_{SYNBRK} as defined below. $T_{SYNBRK} = T_{SYNBRK\_MAX}$ $T_{SYNDEL} = T_{SYNDEL\_MIN}$ $T_{H\_Interbyte} = 0$ 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.2.3	The Test Tool as master sends TST_FRAME_2 with the length of SYNCH BREAK LOW PHASE T_{SYNBRK} as defined below. T_{SYNBRK} = 20bits $T_{SYNDEL} = T_{SYNDEL\_MIN}$ $T_{H\_Interbyte} = 0$ 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.

5.5.3 Length of SYNCH BREAK DELIMITER (DUT as Master)

This test verifies that the DUT as Master transmits the correct length of the SYNCH BREAK DELIMITER T_{SYNDEL}.

TABLE 8 - LENGTH OF SYNCH BREAK DELIMITER TEST PLAN

DUT node as	Master ECU With C = 680pF	
Parameter	V_{ECU} Test Frames	12V TST_FRAME_1
Test Steps	The DUT sends TST_FRAME_1.	
Response	$T_{SYNDEL} \geq T_{SYNDEL\_MIN}$	
Reference	SAE J2602-1, 5.5	

5.5.4 Variation of Length of SYNCH BREAK DELIMITER (DUT as Slave)

This test verifies that the DUT as slave recognizes an ID request with different lengths of SYNCH BREAK DELIMITER T_{SYNDEL}.

The minimum Synch Break Delimiter time is tested in 5.5.2.

TABLE 9A - VARIATION OF LENGTH OF SYNCH BREAK DELIMITER TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.5.4.x (2 cases)
Parameter	V_{ECU} Test Frames	12V TST_FRAME_2, TST_FRAME_6
Test Steps	See Table 9B	
Response	See Table 9B	
Reference	SAE J2602-1, 5.5	

TABLE 9B - VARIATION OF LENGTH OF SYNCH BREAK DELIMITER TEST PLAN

# Test	Test Steps	Response
5.5.4.1	1. The Test Tool as Master sends TST_FRAME_2 with the length of SYNCH BREAK DELIMITER T_{SYNDEL} as defined below. $T_{SYNBRK} = T_{SYNBRK\_MIN}$ $T_{SYNDEL} = T_{SYNDEL\_MAX}$ $T_{H\_Interbyte} = 0$ 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.4.2	1. The Test Tool as master sends TST_FRAME_2 with the length of SYNCH BREAK DELIMITER T_{SYNDEL} as defined below. $T_{SYNBRK} = T_{SYNBRK\_MIN}$ T_{SYNDEL} = 10bits $T_{H\_Interbyte} = 0$ 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.

5.5.5 Length of Header (DUT as Master)

This test verifies that the DUT as Master transmits the correct length of the header T_{HEADER}.

TABLE 10 – LENGTH OF HEADER TEST PLAN

DUT node as	Master ECU With C = 680pF	
Parameter	V_{ECU} Test Frames	12V TST_FRAME_1
Test Steps	The DUT sends TST_FRAME_1.	
Response	$(T_{HEADER\_NOMIINAL} * 0.995) \leq T_{HEADER} \leq T_{HEADER\_MAXIMUM}$	
Reference	SAE J2602-1, 5.5	

5.5.6 Variation of Length of Header (DUT as Slave)

This test verifies that the DUT as slave recognizes an ID request with different lengths of the Header T_{HEADER}.

TABLE 11A - VARIATION OF LENGTH OF HEADER TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.5.6.x (4 cases)
Parameter	V_{ECU} Test Frames	12V TST_FRAME_2, TST_FRAME_6
Test Steps	See Table 11B	
Response	See Table 11B	
Reference	SAE J2602-1, 5.5	

TABLE 11B - VARIATION OF LENGTH OF HEADER TEST PLAN

# Test	Test Steps	Response
5.5.6.1	1. The Test Tool as master sends TST_FRAME_2 with the length of the parts of the header as defined below. $T_{SYNBRK} = T_{SYNBRK\_MIN}$ $T_{SYNDEL} = T_{SYNDEL\_MIN}$ $T_{H\_Interbyte} = 0$ T_{HEADER} = THEADER_NOMINAL 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.6.2	1. The Test Tool as master sends TST_FRAME_2 with the length of the parts of the header as defined below. T_{SYNBRK} = 19bits T_{SYNDEL} = 2bits $T_{H\_Interbyte}$ = 6bits T_{HEADER} = THEADER_MAXIMUM 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.6.3	1. The Test Tool as master sends TST_FRAME_2 with the length of the parts of the header as defined below. T_{SYNBRK} = 15bits T_{SYNDEL} = 3bits $T_{H\_Interbyte}$ = 2bits T_{HEADER} = 40bits 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.
5.5.6.4	1. The Test Tool as master sends TST_FRAME_2 with the length of the parts of the header as defined below. $T_{SYNBRK} = T_{SYNBRK\_MIN}$ $T_{SYNDEL} = T_{SYNDEL\_MIN}$ $T_{H\_Interbyte}$ = 13bits T_{HEADER} = THEADER_MAXIMUM 2. The Test Tool as master sends TST_FRAME_6	The DUT must answer the request.

5.5.7

5.5.8 Length of Frame (DUT as Slave Answering to a Master Request)

5.5.8.1 DUT as Slave

This test verifies that the length of $T_{FRAME\_MAXIMUM}$ is not exceeded by the DUT's in-frame-response space and interbyte spaces.

The header length is set to the maximum $T_{HEADER\_MAXIMUM}$ (worst case).

TABLE 12 – LENGTH OF FRAME (DUT AS SLAVE) TEST PLAN

DUT node as	Slave ECU With C = 220pF	
Parameter	V_{ECU} Test Frames	12V TST_FRAME_2 as defined below, TST_FRAME_6 TST_FRAME_2 parameters: Header size = max Data Frame size = 8 SyncBreak length = 19bits SyncDelimiter length=8bits $T_{HInterbyte}$ = 0
Test Steps	The Test Tool as master sends a request with the maximum length of header, followed by TST_FRAME_6.	
Response	The DUT must answer the request with $T_{FRAME\_NOMINAL} + (T_{Header\_Maximum} - T_{Header\_Nominal}) \le T_{Frame} \le T_{FRAME\_MAXIMUM}$	
Reference	SAE J2602-1, 5.5	

5.5.8.2 DUT as Master with Slave Task

This testz verifies that the length of $T_{FRAME\_MAXIMUM}$ is not exceeded by the DUT's in-frame-response space and interbyte spaces.

TABLE 13 – LENGTH OF FRAME (DUT AS MASTER WITH SLAVE TASK) TEST PLAN

DUT node as	Master ECU with Slave Task With C = 680pF	
Parameter	V_{ECU} Test Frames	12V TST_FRAME_4
Test Steps	The DUT as master sends a request with the maximum length of header, if adjustable.	
Response	The DUT must send the slave response with $T_{FRAME\_NOMINAL} + (T_{Header\_Maximum} - T_{Header\_Nominal}) \le T_{Frame} \le T_{FRAME\_MAXIMUM}$	
Reference	SAE J2602-1, 5.5	

5.6 LIN Product Identification (reference 2.4, LIN 2.0 Diag and Config Specification)

Decided by review by end user.

5.7 Mandatory Node Configuration Requests (reference LIN 2.0 Diagnostics and Configuration Specification)

5.7.1 General Configuration Requirements

5.7.1.1 Slave Execution of Configuration (DUT as Slave)

This test verifies that the slave DUT will perform the $3C command without receiving a $3D request using the Targeted Reset Command.

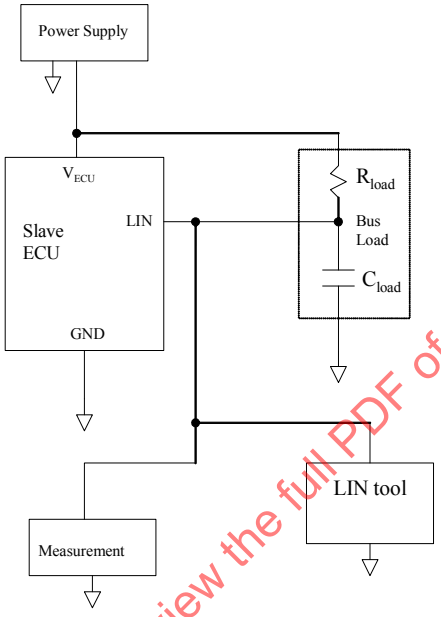

FIGURE 4 - SLAVE EXECUTION OF CONFIGURATION TEST SETUP

TABLE 14A - SLAVE EXECUTION OF CONFIGURATION TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.1.1
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	See Table 14B	
Response	See Table 14B	
Reference	SAE J2602-1, 5.7.1.1	

TABLE 14B - SLAVE EXECUTION OF CONFIGURATION TEST PLAN

# Test	Test Steps	Response
5.7.1.2	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Targeted Reset to the DUT. Do not follow this with a $3D request. 3. Send a slave specific request message ID for DUT without error.	After step 3 the Status Byte returned by the DUT must be (001x xxxx). This verifies that the reset was performed without the device receiving a $3D.

5.7.1.3 Slave Device Configuration Capabilities

Verify NCF is available and complete.

5.7.1.4 Master Configuration Message Pairing

Application software specific.

5.7.2 NAD and Message ID Assignment

5.7.2.1 Slave NAD Assignment

5.7.2.1.1 Devices which have a Hardware Selectable DNN and are also configurable via software must be conformance tested via 5.7.2.1.4. This may require that two devices be tested. The Hardware Selection shall always have a higher priority. Hardware Selectable DNN (DUT as Slave)

This test verifies that the DUT takes on the proper NAD based on the setting of the DNN pins.

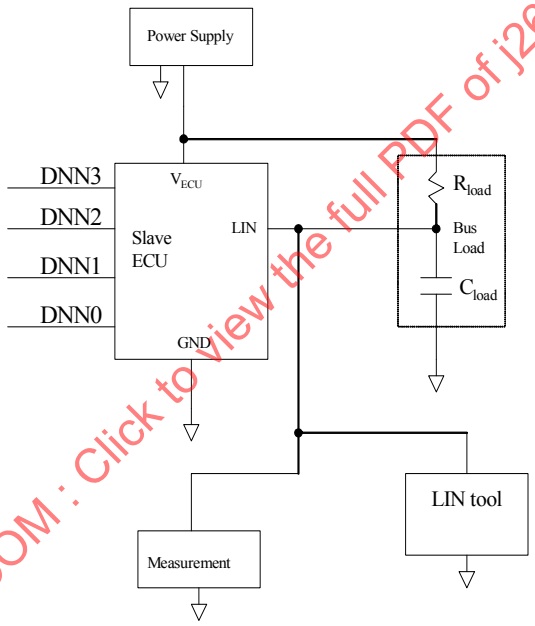

FIGURE 5 - HARDWARE SELECTABLE DNN TEST SETUP

TABLE 15A - HARDWARE SELECTABLE DNN TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.2.1.1.1
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	See Table 15B	
Response	See Table 15B	
Reference	SAE J2602-1, 5.7.2.1	

TABLE 15B - HARDWARE SELECTABLE DNN TEST PLAN

# Test	Test Steps	Response
5.7.2.1.1.1	1. set DNN = $0 2. X = $01 3. Send a $3C Targeted Reset to NAD = X 4. Send a $3D Request. 5. X = X+1 6. If X = $7F, X = X+1 7. If X <= $FF, go to 3 8. set DNN = DNN + 1 9. If DNN <=$D, go to 2	In step 4, the DUT must transmit a response when X = $6(DNN); otherwise, there must be no response sent.

5.7.2.1.2 Fixed DNN (DUT as Slave)

This test verifies the NAD of the DUT.

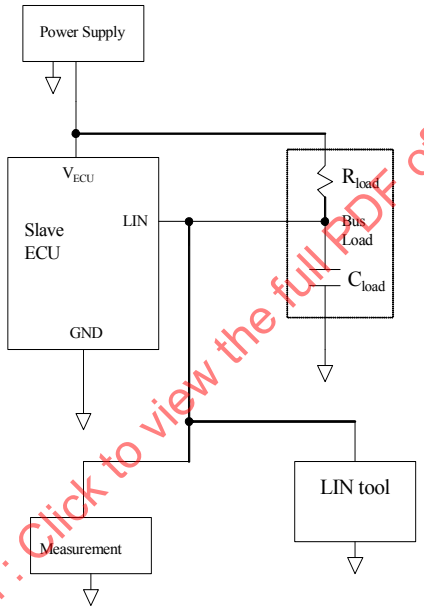

FIGURE 6 - FIXED DNN TEST SETUP

TABLE 16A - FIXED DNN TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.2.1.2.1
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	Perform test with each available fixed NAD See Table 16B	
Response	See Table 16B	
Reference	SAE J2602-1, 5.7.2.1	

TABLE 16B - FIXED DNN TEST PLAN

# Test	Test Steps	Response
5.7.2.1.2.1	1. X = $01 2. Send a $3C Targeted Reset to NAD = X 3. Send a $3D Request. 4. X = X+1 5. If X = $7F, X = X+1 6. If X <= $FF, go to 2	In step 3, the DUT must transmit a response when X = NAD of the DUT; otherwise, there must be no response sent.

5.7.2.1.3 Software Programmable DNN (DUT as Slave)

This test verifies that the DUT takes on the proper NAD based on the programmed DNN.

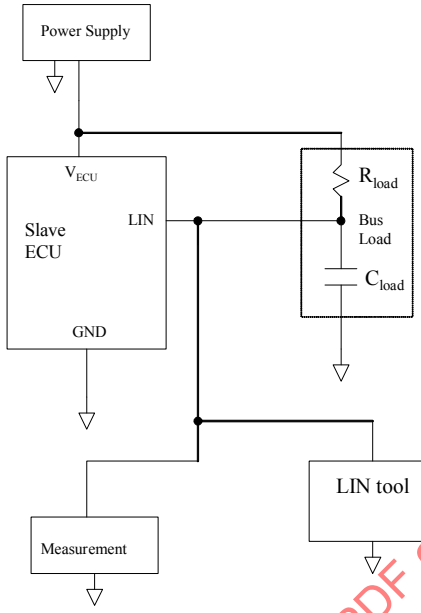

FIGURE 7 - SOFTWARE PROGRAMMABLE DNN TEST SETUP

TABLE 17A - SOFTWARE PROGRAMMABLE DNN TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.2.1.3.1
Parameter	V_{ECU} R_{load} and C_{load} DNN	12V 1 kΩ, 680 pF $F at start of test (uninitialized device)
Test Steps	See Table 17B	
Response	See Table 17B	
Reference	SAE J2602-1, 5.7.2.1	

TABLE 17B - SOFTWARE PROGRAMMABLE DNN TEST PLAN

# Test	Test Steps	Response
5.7.2.1.3.1	1. X = $01 2. Send a $3C Targeted Reset to NAD = X 3. Send a $3D Request. 4. X = X+1 5. If X = $7F, X = X+1 6. If X <= $FF, go to 2 7. set DNN = $E (program by whatever means the DUT uses) 8. X = $01 9. Send a $3C Targeted Reset to NAD = X 10. Send a $3D Request. 11. X = X+1 12. If X = $7F, X = X+1 13. If X <= $FF, go to 9 14. DNN = DNN – 1 (program by whatever means the DUT uses) 15. If DNN >=$0, go to 8	In step 3, the DUT must transmit a response when X = $6F; otherwise, there must be no response sent. In step 10, the DUT must transmit a response when X = $6(DNN); otherwise, there must be no response sent.

5.7.2.1.4 Hardware Selectable DNN and Software Programmable DNN (DUT as Slave)

The following test shall be used to show that the hardware selection cannot be over written by software.

Test setup is as shown in Figure 6.

TABLE 18A - HARDWARE SELECTABLE DNN AND SOFTWARE PROGRAMMABLE DNN TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.2.1.4.1
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	See Table 18B	
Response	See Table 18B	
Reference	SAE J2602-1, 5.7.2.1	

TABLE 18B - HARDWARE SELECTABLE DNN AND SOFTWARE PROGRAMMABLE DNN TEST PLAN

# Test	Test Steps	Response
5.7.2.1.4.1	1. Perform test 5.7.2.1.1.1	As described in test 5.7.2.1.1.1.
5.7.2.1.4.2	1. Perform test 5.7.2.1.3.1	As described in test 5.7.2.1.3.1.
5.7.2.1.4.3	1. set DNN = $0 with hardware selection method 2. Y = $E 3. Attempt to set the DNN to $Y (program by whatever means the DUT uses) 4. X = $01 5. Send a $3C Targeted Reset to NAD = X 6. Send a $3D Request. 7. X = X+1 8. If X = $7F, X = X+1 9. If X <= $FF, go to 5 10. Y = Y-1 11. If Y = DNN, Y= Y-1 12. If Y >= $0, go to 3 13. set DNN = DNN + 1 with hardware selection method 14. If DNN <=$D, go to 2	In step 3, the command is ignored and no response is sent or a negative response is sent. In step 6, the DUT must transmit a response when X = $6(DNN); otherwise, there must be no response sent.

5.7.2.2 Slave Message ID Assignment (DUT as Slave)

This test verifies that the DUT takes on the proper message IDs based on its DNN.

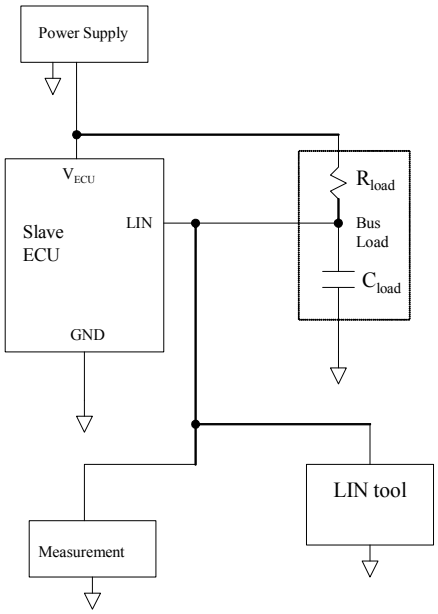

FIGURE 8 - SLAVE MESSAGE ID ASSIGNMENT TEST SETUP

TABLE 19A - SLAVE MESSAGE ID ASSIGNMENT TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.2.2.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	Repeat Test for each NAD in the range $60-$6F that the device is capable of being assigned See Table 19B	
Response	See Table 19B	
Reference	SAE J2602-1, 5.7.2.2	

TABLE 19B - SLAVE MESSAGE ID ASSIGNMENT TEST PLAN

# Test	Test Steps	Response
5.7.2.2.1	1. X = $00 2. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 3. If message ID X is not a request message for the slave, send a message to the slave with an ID of X, 8 data bytes of $00 and a checksum of $00 (incorrect checksum), else jump to 5. 4. Send a slave specific request message to the DUT 5. X = X+1 6. If X >$3B, end 7. else, go to 3.	After step 4, if the message ID sent was a command message ID for the DUT, the Status Byte returned by the DUT must be (101x xxxx), otherwise it must be (000x xxxx).
5.7.2.2.2	1. X = $00 2. If message ID X is not a command message to the slave, send a message header to the slave with an ID of X, else jump to 3. 3. X = X+1 4. If X >$3B, end 5. else, go to 2.	After step 2, if the message ID sent was a request message ID for the DUT, the DUT must respond with the appropriate number of bytes, otherwise the DUT must not send any response.

5.7.2.3 Slave Configuration Messages

1. When using the optional method of configuring nodes as defined in the LIN 2.0 specification, test according to the LIN 2.0 Conformance Test Specification, Node Configuration / Network Management 4.1 and 4.4.

2. When using $3C messages with NADs in the User reserved range of $80 - $FF perform the following test based on information in the node's NCF.

3. When using $3E messages with any NAD perform the following test based on information in the node's NCF.

Send a $3C or $3E message with the appropriate NAD based on the information in the NCF.

$3C NAD

Bit 7 (msb)	6	5	4	3	2	1	Bit 0 (lsb)
1	X	X	X	DNN3	DNN2	DNN1	DNN0

$3E NAD

Bit 7 (msb)	6	5	4	3	2	1	Bit 0 (lsb)
X	X	X	X	DNN3	DNN2	DNN1	DNN0

5.7.2.4 Slave Response Message to Options 2 and 3 in 5.7.2.3

Verify that the $3D Response message that follows each $3C and $3E Command message returns the J2602-1 Status Byte (defined in 5.8.7 of SAE J2602-1) in Data Byte 0. The value of the other seven data bytes is implementation dependent and beyond the scope of this specification.

Tx by Master	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*	*Tx by Slave*
LIN ID	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
$3D	J2602 Status Byte	XX	XX	XX	XX	XX	XX	XX

5.7.2.5 Slave DNN Based Broadcast Messages

Section 5.7.2.2 checks that the slave accepts the proper LIN ID messages.

5.7.3 Targeted Reset

This is tested in 7.1.2.1 or 7.1.2.2.

5.7.4 Broadcast Reset Slave Response (DUT as Slave)

This test verifies that the DUT accepts a Broadcast Reset Command and sets the appropriate bit in the J2602-1 Status Byte.

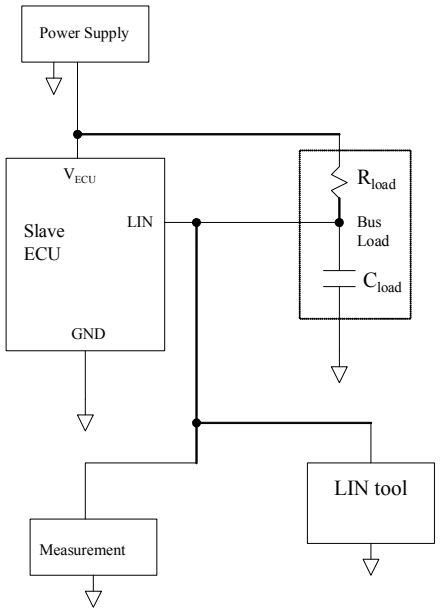

FIGURE 9 - BROADCAST RESET SLAVE RESPONSE TEST SETUP

TABLE 20A - BROADCAST RESET SLAVE RESPONSE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.7.4
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	See Table 20B	
Response	See Table 20B	
Reference	SAE J2602-1, 5.7.4	

TABLE 20B - BROADCAST RESET SLAVE RESPONSE TEST PLAN

# Test	Test Steps	Response
5.7.5	1. Verify no error codes are set in the slave by sending a slave specific request message ID for DUT and checking the Status Byte. There are no error codes set when the most significant bit of the Status Byte is '0'. Repeat until no errors are found. 2. Send a $3C Broadcast Reset to the DUT. Do not follow this with a $3D request as there would not be one. 3. Send a slave specific request message ID for DUT without error.	After step 3 the Status Byte returned by the DUT must be (001x xxxx).

5.8 Master and Slave Message Format

5.8.1 Checksum (reference 2.1.5, LIN 2.0 Protocol Specification)

If this is not correct, no other messaging would work correctly. The tool shall check the checksum in every message sent by the DUT. If the checksum is not correct an error shall be logged.

5.8.2 Signal Consistency (reference 1.2, LIN 2.0 Protocol Specification)

Not a requirement.

5.8.3 Signal Encoding Types (reference 1.1, LIN 2.0 Protocol Specification)

Recommended messaging, not verifiable.

5.8.4 Signal Management

Verified by review of the applicable NCF (Slave ECU) or LDF (Master ECU).

5.8.5 Unused Bits in the Data Field (reference 2.3, LIN 2.0 Protocol Specification)

Informational, not a requirement.

5.8.6 J2602-1 Slave Status Byte

5.8.6.1 Error Field Definition

Verified proper use of Error Field Definition in 5.4.1.

5.8.6.2 Application Information Field

Verified by component/system level testing by the OEM/Tier 1 Supplier.

5.9 Message Types

5.9.1 Availability of Unconditional Frames (reference 2.3.1, LIN 2.0 Protocol Specification)

This is a guideline.

5.9.2 Event Triggered Frames (reference 2.3.2, LIN 2.0 Protocol Specification)

Verified by component/system level testing by the OEM/Tier 1 Supplier.

5.9.2.1 Identifier Assignment (SAE J2602-1 Requirement Resulting from Event Triggered Frame Anomaly)

Verified by component/system level testing by the OEM/Tier 1 Supplier.

5.9.3 Sporadic Frame (reference 2.3.3, LIN 2.0 Protocol Specification)

Verified by component/system level testing by the OEM/Tier 1 Supplier.

5.10 Large Calibration Configuration

5.10.1 Calibrating/Configuring a Slave

This test verifies that the Slave calibration/configuration operates correctly

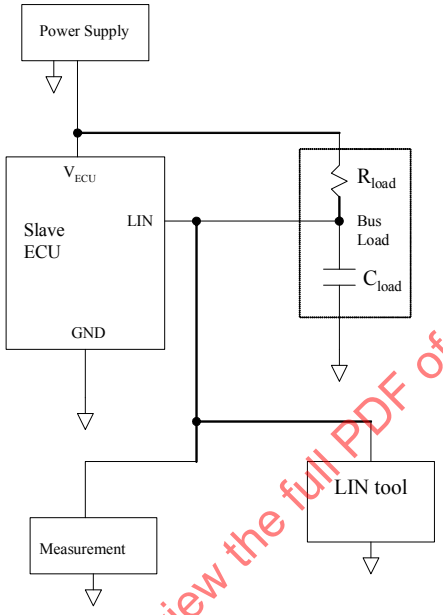

FIGURE 10 – CALIBRATING/CONFIGURING A SLAVE TEST SETUP

TABLE 21A - CALIBRATING/CONFIGURING A SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.10.1
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	Requires an uncalibrated/configured Slave ECU. See Table 21B	
Response	See Table 21B	
Reference	SAE J2602-1, 5.10.1	

TABLE 21B - CALIBRATING/CONFIGURING A SLAVE TEST PLAN

# Test	Test Steps	Response
5.10.1.	1. Verify the slave is not calibrated by sending a slave specific request message ID for DUT and checking the Status Byte. 2. Send a known good calibration/configuration file to the slave. 3. Verify the slave is calibrated by sending a slave specific request message ID for DUT and checking the Status Byte.	After step 1 APINFO4 bit in the SAE J2602 Status byte is set indicating that the slave is not calibrated After step 3 APINFO4 bit in the SAE J2602-1 Status byte is cleared indicating that the slave is calibrated

5.10.2 Slave Part Number Reporting

Verify that the Slave Part Number Reporting operates correctly

Test Setup as shown in Figure 10.

TABLE 22A – SLAVE PART NUMBER REPORTING TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 5.10.2
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	Requires a calibrated/configured Slave ECU. See Table 22B	
Response	See Table 22B	
Reference	SAE J2602-1, 5.10.2	

TABLE 22B – SLAVE PART NUMBER REPORTING TEST PLAN

# Test	Test Steps	Response
5.10.3	1.Power up the Slave and begin transmitting the part Number reporting schedule table to the slave. 2.Evaluate the part number reported in the log file of the bus analyzer	After step 1 verify that the schedule table completed without errors After step 2 verify that the correct part number was retrieved from the Slave

5.11 Small Calibration Configuration

This test verifies that the slave node can be configured correctly. This test also verifies that the slave can recognize an incorrect calibration file and report this properly when queried. Finally, it verifies that a correct file will be accepted after an erroneous file has been sent.

The following Artifacts are required to perform the testing described in this section.
Artifact #1: Valid calibration file for the slave
Artifact #2: Calibration file with modified data (so that the file checksum is incorrect)
Artifact #3: Calibration file with modified data length (# of bytes < correct #) (checksum will not be in error if the calibration file length modification was accomplished by deleting a frame of “fill” bytes.)
Tool: method for transmitting a series of data bytes in a sequence beginning at an arbitrary ID of length N. Then transmit response ID for Calibration Part Number frame.

TABLE 23A - CALIBRATING/CONFIGURING A SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test cases 5.11.1 - 5.11.5
Parameter	V_{ECU} R_{load} and C_{load}	12V 1 kΩ, 680 pF
Test Steps	Requires an uncalibrated/configured Slave ECU. See Table 23B	
Response	See Table 23B	
Reference	SAE J2602-1, 5.11.1	

TABLE 23B - CALIBRATING/CONFIGURING A SLAVE TEST PLAN

# Test	Test Steps	Response
5.11.1	1. Verify that the slave is uncalibrated by sending the response frame request for the Calibration Part Number response. 2. Send Artifact #1 as described above. 3. Verify the slave is configured by sending the response frame request for the Calibration Part Number response.	After step 1 APINFO3 bit in the SAE J2602-1 Status byte is set indicating that the slave is not calibrated and that the Calibration Part Number response identifies the “loaded” part number to be $00 $00 $00 $00. After step 3 APINFO3 bit in the SAE J2602-1 Status byte is cleared indicating that the slave is calibrated and that the Calibration Part Number and End Item part number match what was sent in Artifact #1.
5.11.2	1. Send Artifact #2 as described above. 2. Verify the slave is not configured and rejected the erroneous file by sending the response frame request for the Calibration Part Number response.	After step 2 APINFO3 bit in the SAE J2602-1 Status byte is set indicating that the slave is not calibrated and that the Calibration Part Number response identifies the “loaded” part number to be $00 $00 $00 $00.
5.11.3	1. Send Artifact #3 as described above. 2. Verify the slave is not configured and rejected the erroneous file by sending the response frame request for the Calibration Part Number response.	After step 2 APINFO3 bit in the SAE J2602-1 Status byte is set indicating that the slave is not calibrated and that the Calibration Part Number response identifies the “loaded” part number to be $00 $00 $00 $00.
5.11.4	1. Send Artifact #1 as described above. 2. Verify the slave is configured by sending the response frame request for the Calibration Part Number response.	After step 2 APINFO3 bit in the SAE J2602-1 Status byte is cleared indicating that the slave is calibrated and that the Calibration Part Number and End Item part number match what was sent in Artifact #1.

6. J2602-1 API REQUIREMENTS

6.1 Master Node Configuration API

Not externally verifiable, requires a software review.

6.2 Diagnostic Transport Layer API

Not a requirement.

6.3 Additional API Requirements

Not externally verifiable, requires a software review.

7. J2602-1 BUS OPERATION

The physical layer is responsible for providing a method of transferring digital data symbols (1's and 0's) to the communication medium. The physical layer interface is a single wire, vehicle battery referenced bus, with low side voltage drive.

7.1 Normal Communication Mode and Transmission Rate

7.1.1 Master Node Bit Time Measurement

This test verifies the bit time of the Master DUT is within the specified range under maximum and minimum bus loading conditions.

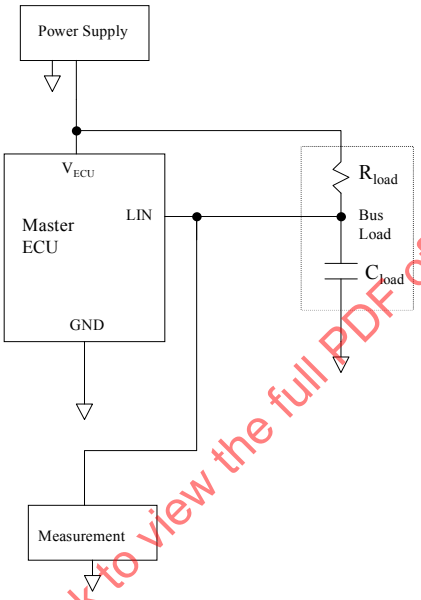

FIGURE 11 - MASTER NODE BIT TIME MEASUREMENT TEST SETUP

TABLE 24A - MASTER NODE BIT TIME MEASUREMENT TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 7.1.1.x (4 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 24B
Test Steps	1. Sum = 0 2. Measure time from r-d edge at start bit of sync byte to final r-d edge of the sync byte (8 bit times) → t. Take measurements at 0.6 * V_{ECU} → 7.2V. 3. Sum = Sum + t 4. Repeat steps 2 and 3 20 times 5. Average bit time = Sum / 20 / 8	
Response	See Table 24B	
Reference	SAE J2602-1, 7.1	

TABLE 24B - MASTER NODE BIT TIME MEASUREMENT TEST PLAN

# Test		R_{load}	C_{load}	Response
7.1.1.1	(min tau with 15 slaves + wiring)	1.33 kΩ	1.59 nF	The average bit time shall be between (96 µs (1+/- (0.005 – aging factor of clock)))
7.1.1.2	(max tau with 15 slaves + wiring)	4.00 kΩ	5.5 nF	The average bit time shall be between (96 µs (1+/- (0.005 – aging factor of clock)))
7.1.1.3	(min tau with 1 slave + wiring)	20 kΩ	889 pF	The average bit time shall be between (96 µs (1+/- (0.005 – aging factor of clock)))
7.1.1.4	(max tau with 1 slave + wiring)	60 kΩ	4.35 nF	The average bit time shall be between (96 µs (1+/- (0.005 – aging factor of clock)))

7.1.2 Slave Node Bit Time Measurement

This test verifies the bit time of the Slave DUT is within the specified range under maximum and minimum bus loading conditions. This test also verifies that the Slave DUT can respond to a $3D request immediately following a $3C Targeted Reset command. (Requirement from 5.7.3 of SAE J2602-1.)

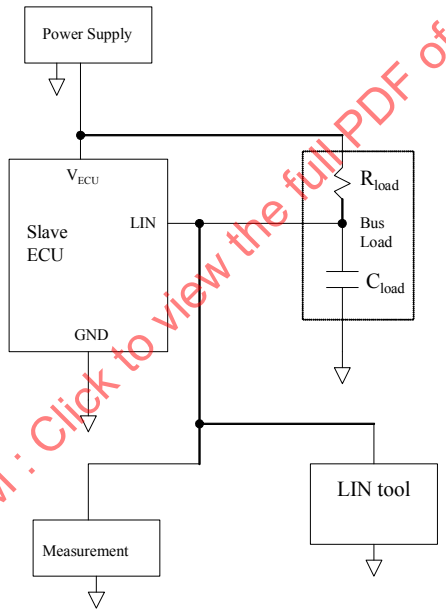

FIGURE 12 - SLAVE NODE BIT TIME MEASUREMENT TEST SETUP

7.1.2.1 Fixed Clock Slave Node

TABLE 25A - SLAVE NODE BIT TIME MEASUREMENT - FIXED CLOCK TEST PLAN

DUT node as	Slave ECU With C = 220pF nominal	Test case 7.1.2.1.x (4 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 25B
Test Steps	1. Sum = 0 2. LIN tool transmits a Targeted Reset to the DUT 3. LIN tool transmits a $3D header to the DUT. The break character of the $3D header shall begin 20 ms after the start of the break character for the $3C Targeted Reset. 4. Measure time from r-d edge at start bit of NAD to final r-d edge of the NAD (0xxxx01101) (8 bit times) ➔ t Take measurements at 0.6 * V_{ECU} → 7.2V. 5. Sum = Sum + t 6. Repeat steps 2 -5 20 times 7. Average bit time = Sum / 20 / 8	
Response	See Table 25B	
Reference	SAE J2602-1, 7.1	

TABLE 25B - SLAVE NODE BIT TIME MEASUREMENT - FIXED CLOCK TEST PLAN

# Test		R_{load}	C_{load}	Response
7.1.2.1.1	(min tau with 15 slaves + wiring)	552 Ω	1.64 nF	The average bit time shall be between (96 µs (1+/- (0.015 – aging factor of clock)))
7.1.2.1.2	max tau with 15 slaves + wiring)	875 Ω	5.5 nF	The average bit time shall be between (96 µs (1+/- (0.015 – aging factor of clock)))
7.1.2.1.3	min tau with 1 slave + wiring)	900 Ω	889 pF	The average bit time shall be between (96 µs (1+/- (0.015 – aging factor of clock)))
7.1.2.1.4	(max tau with 1 slave + wiring)	1.1 k Ω	4.35 nF	The average bit time shall be between (96 µs (1+/- (0.015 – aging factor of clock)))

7.1.2.2 Autobauding Slave Node

TABLE 26A - SLAVE NODE BIT TIME MEASUREMENT - AUTOBAUDING CLOCK TEST PLAN

DUT node as	Slave ECU With C = 220pF nominal	Test case 7.1.2.2.x (4 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 26B
Test Steps	1. SumM = 0, SumS = 0 2. LIN tool transmits a Targeted Reset to the DUT 3. LIN tool transmits a $3D header to the DUT. The break character of the $3D header shall begin 20 ms after the start of the break character for the $3C Targeted Reset. 4. Measure time from r-d edge at start bit of sync byte to final r-d edge of the sync byte (8 bit times) ➔ t. Take measurements from 1 V below peak recessive voltage. 5. SumM = SumM + t 6. Measure time from r-d edge at start bit of NAD byte to final r-d edge of the NAD byte (0xxxx01101) (8 bit times) ➔ y Take measurements from 1 V below peak recessive voltage. 7. SumS = SumS + y 8. Repeat steps 2 -5 20 times 9. Average Master bit time = SumM / 20 / 8 10. Average DUT bit time = SumS / 20 /8	
Response	See Table 26B	
Reference	SAE J2602-1, 7.1	

TABLE 26B - SLAVE NODE BIT TIME MEASUREMENT - AUTOBAUDING CLOCK TEST PLAN

# Test	R_{load}	C_{load}	Response
7.1.2.2.1 (min tau with 15 slaves + wiring)	552 Ω	1.64 nF	SumM (0.98) ≤ SumS ≤ SumM (1.02)
7.1.2.2.2 (max tau with 15 slaves + wiring)	875 Ω	5.5 nF	SumM (0.98) ≤ SumS ≤ SumM (1.02)
7.1.2.2.3 (min tau with 1 slave + wiring)	900 Ω	889 pF	SumM (0.98) ≤ SumS ≤ SumM (1.02)
7.1.2.2.4 (max tau with 1 slave + wiring)	1.1 k Ω	4.35 nF	SumM (0.98) ≤ SumS ≤ SumM (1.02)

7.2 Sleep/Wake Mode in Master and Slave

Use the following messages for the Test Frames called out in these sections:

TABLE 27 - TEST FRAME ASSIGNMENTS

TST_Frame	Requirements for the Test Frame
TST_FRAME_1	Any frame sent by the master
TST_FRAME_2	Targeted Reset
TST_FRAME_3	Not Used
TST_FRAME_4	Device Specific Frame
TST_FRAME_5	Not Used
TST_FRAME_6	Slave Response Command Frame, Identifier = 0x3D
TST_FRAME_7	Not Used
TST_FRAME_8	Not Used
TST_FRAME_9	Command Frame Sleep Request, Identifier = 0x3C, NAD = 0x00

7.2.1 Wake-up of Master and Slave (reference 5.1, LIN 2.0 Protocol Specification)

7.2.1.1 Wake-up Request to the Master (DUT as Master)

This test verifies the ability of the Master node to receive a wake-up request and to process it upon reception.

TABLE 28A – MASTER NODE WAKE-UP RECEPTION

DUT node as	Master ECU With C = 680pF	Test Case 7.2.1.1.x (4 Cases)
Parameter	V_{ECU}	12V
Test Steps	See Table 28B	
Response	See Table 28B	
Reference	SAE J2602-1, 7.2.1	

TABLE 28B – MASTER NODE WAKE-UP RECEPTION

# Test	Test Steps	Response
7.2.1.1.1	1. The DUT is in the sleep mode 2. The Test Tool as slave sends a wakeup request for 29µS.	The DUT must not wake-up and transmit its messages.
7.2.1.1.2	1. The DUT is in the sleep mode 2. The Test Tool as slave sends a wakeup request for 250µS.	The DUT must receive the wake-up request and initialize the start up routine. The DUT must send out the frame headers to find the root cause for the request between 100 and 110 ms of the dominant to recessive edge of the wake-up.
7.2.1.1.3	1. The DUT is in the sleep mode 2. The Test Tool as slave sends a wakeup request for 1mS.	The DUT must receive the wake-up request and initialize the start up routine. The DUT must send out the frame headers to find the root cause for the request between 100 and 110 ms of the dominant to recessive edge of the wake-up.
7.2.1.1.4	1. The DUT is in the sleep mode 2. The Test Tool as slave sends a wakeup request for 5mS.	The DUT must receive the wake-up request and initialize the start up routine. The DUT must send out the frame headers to find the root cause for the request between 100 and 110 ms of the dominant to recessive edge of the wake-up.

7.2.1.2 Wake-Up request to the Slave (DUT as Slave)

This test verifies the ability of the Slave node to receive a wake-up request and to process it upon reception.

TABLE 29A – SLAVE NODE WAKE-UP RECEPTION

DUT node as	Slave ECU With C = 220pF	Test Case 7.2.1.2.x (4 cases)
Parameter	V_{ECU}	12V
Test Steps	See Table 29B	
Response	See Table 29B	
Reference	SAE J2602-1, 7.2.1	

TABLE 29B – SLAVE NODE WAKE-UP RECEPTION

# Test	Test Steps	Response
7.2.1.2.1	1. The DUT is in the sleep mode 2. The Test Tool as Master sends a wakeup request for 29µS. 3. Wait for 100ms 4. Send a $3C Targeted Reset to the DUT 5. Send a $3D Response	After Step 5 the DUT must not transmit any of its messages.
7.2.1.2.2	1. The DUT is in the sleep mode 2. The Test Tool as Master sends a wakeup request for 250µS. 3. Wait for 100ms 4. Send a $3C Targeted Reset to the DUT 5. Send a $3D Response	After Step 2 the DUT must receive the wake-up request and initialize the start up routine. After Step 5 the DUT must transmit thethe $3D response data.
7.2.1.2.3	1. The DUT is in the sleep mode 2. The Test Tool as Master sends a wakeup request for 1mS. 3. Wait for 100ms 4. Send a $3C Targeted Reset to the DUT 5. Send a $3D Response	After Step 2 the DUT must receive the wake-up request and initialize the start up routine. After Step 5 the DUT must transmit the $3D response data.
7.2.1.2.4	1. The DUT is in the sleep mode 2. The Test Tool as Master sends a wakeup request for 5mS5mS. 3. Wait for 100ms 4. Send a $3C Targeted Reset to the DUT 5. Send a $3D Response	After Step 2 the DUT must receive the wake-up request and initialize the start up routine. After Step 5 the DUT must transmit the $3D response datadata.

7.2.1.3 Transmit a Wake-Up Request (DUT as a Slave or Master with Slave Task)

This test verifies the ability of a slave node to transmit a wake-up request.

This test is only applicable to slaves which have wake-up inputs that will generate a LIN bus wake-up.

TABLE 30 – SLAVE NODE (OR MASTER NODE WITH SLAVE TASK) WAKE-UP TRANSMISSION

DUT node as	Slave ECU with C = 220pFOR Master ECU with Slave Task With C = 680pF	
Parameter	V_{ECU}	12V
Test Steps	1.The DUT is in the sleep mode 2.Activate a local wake-up input in the DUT so that a wake-up is generated	
Response	The wakeup pulse length must be 250µs < t < 5mS	
Reference	SAE J2602-1, 7.2.1	

7.2.1.4 Repeat Wake-Up request when no response by Master (DUT as a Slave)

This test verifies the ability of the slave node to resend the wake-up request when there is no response from a master after a wake-up request.

This test is only applicable to slaves which have wake-up inputs that will generate a LIN bus wake-up.

TABLE 31A – SLAVE NODE WAKE-UP RE-TRANSMISSION

DUT node as	Slave ECU With C = 220pF	
Parameter	V_{ECU}	12V
Test Steps	See Table 31B	
Response	See Table 31B	
Reference	SAE J2602-1, 7.2.1	

TABLE 31B – SLAVE NODE WAKE-UP RE-TRANSMISSION

# Test	Test Steps	Response
7.2.1.4.1	1. The DUT is in the sleep mode 2. Activate a local input in the DUT that generates a Wake-up pulse on the LIN Bus.	After Step 2 the DUT must transmit the wake-up requests. 150ms < Twu1 < 300ms 1.5s < Twu2 < 3s After the transmission of the 6th Wake-up pulse monitor the bus for 4 more s to check whether the DUT transmits any more wake-up pulse.
7.2.1.4.2	Repeat all steps of 7.2.1.4.1. one more time	Same as above

7.2.1.5 Wake-Up Request from Slave followed by a Frame Header from Master (DUT as Slave)

This test verifies the behavior of the slave on receiving the Frame Header from the Master for a Wake-Up request.

This test is only applicable to slaves which have wake-up inputs that will generate a LIN bus wake-up.

TABLE 32A – SLAVE NODE WAKE-UP REQUEST

DUT node as	Slave ECU With C = 220pF	
Parameter	V_{ECU}	12V
Test Steps	See Table 32B	
Response	See Table 32B	
Reference	SAE J2602-1, 7.2.1	

TABLE 32B - SLAVE NODE WAKE-UP REQUEST

# Test	Test Steps	Response
7.2.1.5.1	1. The DUT is in the sleep mode 2. Activate a local wake-up input in the DUT 3. Wait for 100ms 4. Send TST_FRAME_2 to the DUT 5. Send TST_FRAME_6	After Step 2 the DUT must transmit a Wake-Up request on the LIN bus. After Step 4 the DUT must stop the transmission of the Wake-Up pulse After Step 5 the DUT must answer TST_FRAME_6

7.2.2 Go To Sleep (reference 5.2, LIN 2.0 Protocol Specification)

These tests verify that the slave goes to sleep under the specified conditions.

7.2.2.1 Send Command Frame “Sleep Mode Command” (DUT as Master)

This test verifies the ability of the Master node to send command frames; the “Sleep Mode Command” is used for this testing.

TABLE 33 - MASTER NODE COMMAND TRANSMIT

DUT node as	Master ECU With C = 680pF	
Parameter	V_{ECU}	12V
Test Steps	1.The DUT is initialized 2.The Master must be set up so it will transition the LIN bus into the sleep state 3.The DUT transmits TST_FRAME_9	
Response	The DUT must send the frame without failure and the first data byte must be 0x00. The DUT must not send any more messages.	
Reference	SAE J2602-1, 7.2.2	

7.2.2.2 Receive Command Frame “Sleep Mode Command" (DUT as Slave)

This test verifies the ability of the slave node to receive a command frame. The command frame type 'Sleep Mode Command' is checked in this test, this frame is used to broadcast the sleep mode to all bus nodes.

TABLE 34 – SLAVE NODE COMMAND RECEIVE

DUT node as	Slave ECU With C = 220pF	
Parameter	V_{ECU}	12V
Test Steps	The Test Tool, as a Master, sends TST_FRAME_9 on the bus.	
Response	The current drawn by the DUT must go to its specified quiescent current level within 10 sec unless otherwise specified in the component specification.	
Reference	SAE J2602-1, 7.2.2	

7.2.2.3 Sleep Mode after Bus Idle (DUT as Slave)

This test verifies the ability of the slave node to enter the sleep mode when the bus is idle for more than 4 s.

TABLE 35A – SLAVE NODE SLEEP ON BUS IDLE

DUT node as	Slave ECU With C = 220pF	Test Case 7.2.2.3.x (3 Cases)
Parameter	V_{ECU}	12V
Test Steps	See Table 35B	
Response	See Table 35B	
Reference	SAE J2602-1, 7.2.2	

TABLE 35B – SLAVE NODE SLEEP ON BUS IDLE

# Test	Test Steps	Response
7.2.2.3.1	1. The DUT is in the sleep mode 2. Send a wake-up pulse from the test tool. 3. Wait for 100ms 4. The test tool shall send TST_FRAME_2 followed by the TST_FRAME_6. 5. The test tool shall send the header of TST_FRAME_2. 6. Wait for 4 s	After Step 2 the DUT must wake-up and enter the initialization routine. After Step 4 the DUT must send the response data to TST_FRAME_6. After Step 6 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS.
7.2.2.3.2	1. The DUT is in the sleep mode 2. Send a wake-up pulse from the test tool. 3. Wait for 100ms 4. The test tool shall send TST_FRAME_2 followed by TST_FRAME_6. 5. The test tool shall send the header of TST_FRAME_2 with the first data byte. 6. Wait for 4 s	After Step 2 the DUT must wake-up and enter the initialization routine. After Step 4 the DUT must send the response data to TST_FRAME_6. After Step 6 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS.
7.2.2.3.3	1. Power on the DUT 2. Ensure that there is no message traffic on the bus. 3. Wait for 4 s	After Step 3 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS.

7.2.2.4 Sleep Mode Entered with LIN Bus Shorted to Ground (DUT as Slave)

TABLE 36A – SLAVE NODE SLEEP WITH LIN BUS SHORT TO GROUND

DUT node as	Slave ECU With C = 220pF	
Parameter	V_{ECU}	12V
Test Steps	See Table 36B	
Response	See Table 36B	
Reference	SAE J2602-1, 7.2.2	

TABLE 36B – SLAVE NODE SLEEP WITH LIN BUS SHORT TO GROUND

# Test	Test Steps	Response
7.2.2.4.1	1. The DUT is in the active mode 2. The test tool shall send TST_FRAME_2 followed by TST_FRAME_6. 3. Short the LIN bus to ground 4. Wait for 4 s 5. Wait for 120 s 6. Remove the bus short to ground	After Step 2 the DUT must send the response data to TST_FRAME_6. After Step 4 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS
7.2.2.4.2	1. The DUT is in the active mode 2. The test tool shall send TST_FRAME_2 followed by TST_FRAME_6. 3. The test tool shall send the header of TST_FRAME_2 only. 4. Short the LIN bus to ground 5. Wait 4 s 6. Wait for 120 s 7. Remove the bus short to ground	After Step 2 the DUT must send the response data to TST_FRAME_6. After Step 5 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS.
7.2.2.4.3	1. The DUT is in the active mode 2. The test tool shall send TST_FRAME_2 followed by TST_FRAME_6. 3. The test tool shall send the header of TST_FRAME_2 with the first data byte. 4. Short the LIN bus to ground 5. Wait 4 s 6. Wait for 120 s 7. Remove the bus short to ground	After Step 2 the DUT must send the response data to TST_FRAME_6. After Step 5 the current drawn by the DUT must go to the quiescent current level specified in the component specification within 60 s unless otherwise specified in the CTS.

7.3 LIN Controller Clock Tolerance

See data sheet and clock divide error.

Document oscillator type, tolerance (Initial, temp, aging), PLL Drift over 6uS and LIN controller bit timing accuracy (inexact bit time due to non-integer clock frequency).

7.4 Bus Electrical Parameters

This section describes the bus electrical voltage level parameters required by devices that drive and receive signals on the LIN bus.

7.4.1 LIN Bus Signals and Loading Requirements

TABLE 37 - LIN BUS SIGNALS AND LOADING REQUIREMENTS

Parameter	Symbol	Min.	Typ.	Max.	Units
Output High Voltage	V_{oh}	0.8 $V_{batt\ IC}$		$V_{batt\ IC}$	V
High Voltage (Recessive) Input Threshold	V_{ih}	0.47 $V_{batt\ IC}$		0.6 $V_{batt\ IC}$	V
Output Low Voltage	V_{ol}	0.0		0.2 $V_{batt\ IC}$	V
Low Voltage (Dominant) Input Threshold	V_{il}	0.4 $V_{batt\ IC}$		0.53 $V_{batt\ IC}$	V
Input Threshold Hysteresis (V_{ih} - V_{il}) [6]	V_{HYS}	0.07 $V_{batt\ IC}$		0.175 $V_{batt\ IC}$	V
LIN bus to Ground Isolation Resistance	$V_{L\text{-}G\ Iso}$	500 K			Ω
Slave Termination Resistance	R_S	20 000	30 000	60 000	Ω
$t_{REC(MAX)} - t_{DOM(MIN)}$ [5]	$T_{r\text{-}d\ max}$	-		15.9	µsec
$t_{DOM(MAX)} - t_{REC(MIN)}$ [5]	$T_{d\text{-}r\ max}$	-		17.28	µsec

7.4.1.1 Master Node V_{oh} and V_{ol} Levels Measurement

This test verifies the dominant and recessive output voltages of the Master DUT are within the specified range under maximum and minimum supply voltages.

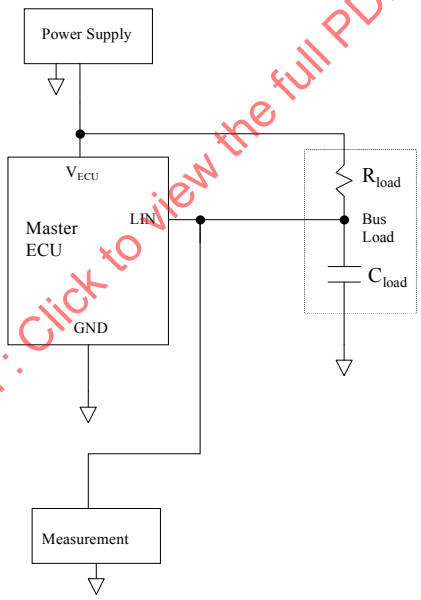

FIGURE 13 - MASTER NODE V_{OH} AND V_{OL} LEVELS MEASUREMENT TEST SETUP

TABLE 38A - MASTER NODE V_{OH} AND V_{OL} LEVELS MEASUREMENT TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 7.4.1.1.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 38B Set to 4.0 KΩ Set to 5.5 nF
Test Steps	For each entry 1. Master Node transmits any message 2. Logic '1' and Logic '0' voltages are measured during the synch byte 3. Repeat steps 1-2 20 times	
Response	See Table 38B	
Reference	SAE J2602-1, 7.4.1	

TABLE 38B - MASTER NODE V_{OH} AND V_{OL} LEVELS MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.1.1	8.0 V	Measure Logic 1 and Logic 0 of the Synch Byte Field as shown in Figure 14. Logic 1 ≥ 5.6 V, Logic 0 ≤ 1.6 V
7.4.1.1.2	18.0 V	Measure Logic 1 and Logic 0 of the Synch Byte Field as shown in Figure 14. Logic 1 ≥ 13.6 V, Logic 0 ≤ 3.6 V.

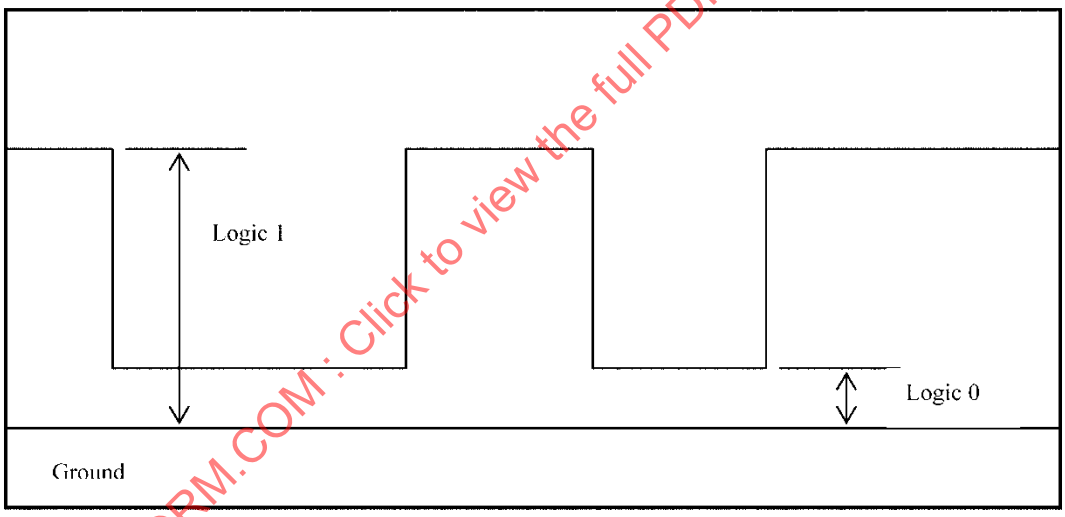

FIGURE 14 - LOGIC LEVEL VOLTAGE MEASUREMENT DESCRIPTION

7.4.1.2 Slave Node V_{oh} and V_{ol} Levels Measurement

This test verifies the dominant and recessive output voltages of the Slave DUT are within the specified range under maximum and minimum supply voltages.

TABLE 39A - SLAVE NODE V_{OH} AND V_{OL} LEVELS MEASUREMENT TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.4.1.2.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 39B Set to 875 Ω Set to 5.5 nF
Test Steps	1. LIN tool transmits a Targeted Reset to the DUT 2. LIN tool transmits a $3D header to the DUT 3. Measure Logic '1' and Logic '0' voltages during the RSID byte in the DUT response. 4. Repeat steps 1-3 20 times.	
Response	See Table 39B	
Reference	SAE J2602-1, 7.4.1	

TABLE 39B - SLAVE NODE V_{OH} AND V_{OL} LEVELS MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.2.1	8.0 V	Measure Logic 1 and Logic 0 of the RSID byte as shown in Figure 14 Logic 1 ≥ 5.6 V, Logic 0 ≤ 1.6 V
7.4.1.2.2	18.0 V	Measure Logic 1 and Logic 0 of the RSID Byte as shown in Figure 14. Logic 1 ≥ 13.6 V, Logic 0 ≤ 3.6 V.

7.4.1.3 Master Node V_{ih} Level Measurement

This test verifies the recessive input threshold of the Master DUT is within the specified range under maximum and minimum supply voltages.

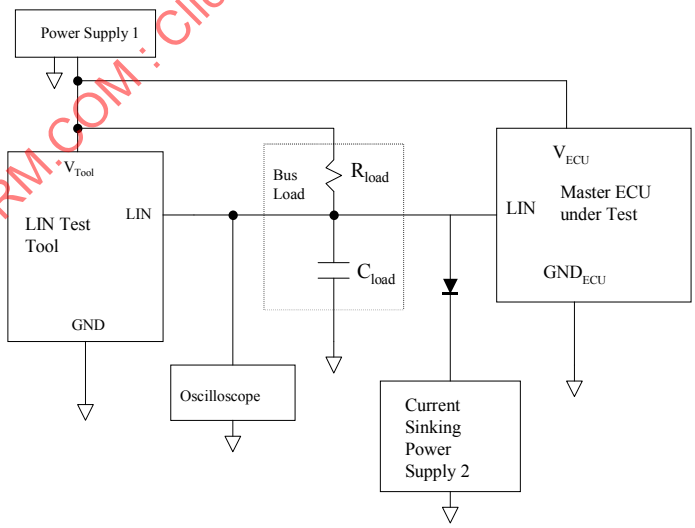

FIGURE 15 - MASTER NODE V_{IH} LEVEL MEASUREMENT TEST SETUP

TABLE 40A - MASTER NODE V_{IH} LEVEL MEASUREMENT TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 7.4.1.3.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 40B Set to 4.0 KΩ Set to 5.5 nF
Test Steps	For each entry in Table 40B: 1. Set Power Supply 2 so that the maximum LIN bus voltage is 0.8*V_{ECU} 2. Configure and allow the Master to enter sleep mode 3. Tool sends wakeup command to the master. If the master wakes up within 100 ms (indicated by the master transmitting a message) go to step 4, if not go to step 5 4. Lower Power Supply 2 by 0.1 Volt and repeat from step 2 5. Record the last Power Supply 2 setting where the master Woke up	
Response	See Table 40B	
Reference	SAE J2602-1, 7.4.1	

TABLE 40B - MASTER NODE V_{IH} LEVEL MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.3.1	8.0 V	The Master must transition from waking to not waking in response to the wake up message when: 4.8 V ≥ Recessive LIN bus voltage ≥ 3.29 V
7.4.1.3.2	18.0 V	The Master must transition from waking to not waking in response to the wake up message when: 10.8 V ≥ Recessive LIN bus voltage ≥ 7.99 V

NOTE: The thresholds observed in this test may not be the normal mode thresholds, but may be special sleep mode thresholds. The transceiver used in the Master should also be tested on its own or in a slave device to ensure compliance with this spec item.

7.4.1.4 Slave Node V_{ih} Level Measurement

This test verifies the recessive input threshold of the Slave DUT is within the specified range under maximum and minimum supply voltages.

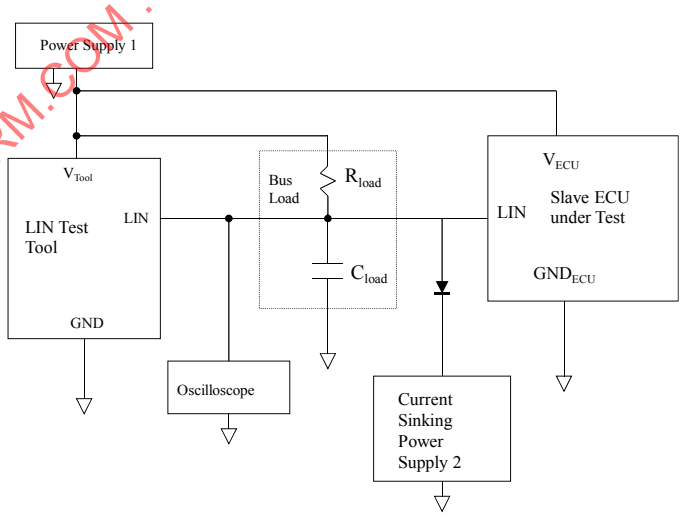

FIGURE 16 - SLAVE NODE V_{IH} LEVEL MEASUREMENT TEST SETUP

TABLE 41A - SLAVE NODE V_{IH} LEVEL MEASUREMENT TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.4.1.4.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 41B Set to 875 Ω Set to5.5 nF
Test Steps	For each entry in Table 41B: 1. Set Power Supply 2 so that the maximum LIN bus voltage is 0.8*V_{ECU} 2. LIN tool transmits a Targeted Reset to the DUT 3. LIN tool transmits a $3D header to the DUT 4. If the slave sends a response to the header go to step 5, if not go to step 6 5. Lower Power Supply 2 by 0.1 Volt and repeat from step 2 6. Record the last Power Supply 2 setting where the Slave responded to the $3D header 7. Repeat steps 1 – 6 20 times	
Response	See Table 41B	
Reference	SAE J2602-1, 7.4.1	

TABLE 41B - SLAVE NODE V_{IH} LEVEL MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.4.1	8.0 V	The Slave must transition from responding to not responding to the $3D header when: 4.8 V ≥ Recessive LIN bus voltage ≥ 3.29 V
7.4.1.4.2	18.0 V	The Slave must transition from responding to not responding to the $3D header when: 10.8 V ≥ Recessive LIN bus voltage ≥ 7.99 V

7.4.1.5 Master Node V_{il} Level Measurement and Input Threshold Hysteresis (V_{ih} - V_{il})

This test verifies the dominant input threshold of the Master DUT is within the specified range under maximum and minimum supply voltages.

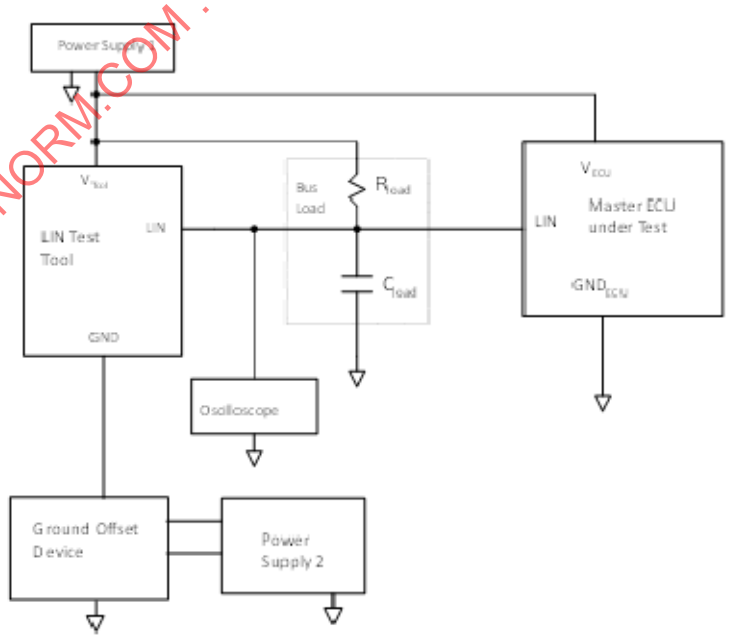

FIGURE 17 - MASTER NODE V_{IL} LEVEL MEASUREMENT TEST SETUP

NOTE: Power Supply 2 is optional and may not be needed if the Ground Offset Device is a Potentiometer.

TABLE 42A - MASTER NODE V_{IL} LEVEL MEASUREMENT TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 7.4.1.5.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 42B Set to 4.0 KΩ Set to 5.5 nF
Test Steps	For each entry in Table 42B: 1. Set Power Supply 2 to 0.2*V_{ECU} or adjust Ground Offset Device to obtain the desired voltage 2. Configure and allow the Master to enter sleep mode 3. Send wakeup command to the master. If the master wakes up within 100 ms (indicated by the master transmitting a message) go to step 4, if not go to step 5 4. Increase Power Supply 2 by 0.1 V or adjust Ground Offset Device to obtain the desired voltage and repeat step 2 5. Record the last Power Supply 2 setting where the master Woke up 6. Repeat steps 1 – 5 20 times 7. Calculate Input Threshold Hysteresis (V_{ih} - V_{il}) with average of values from section 7.4.1.3 and 7.4.1.5.	
Response	See Table 42B	
Reference	SAE J2602-1, 7.4.1	

TABLE 42B - MASTER NODE V_{IL} LEVEL MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.5.1	8.0 V	The Master must transition from waking to not waking in response to the wake up message when: 4.24 V ≥ Power Supply 2 ≥ 2.8 V
7.4.1.5.2	18.0 V	The Master must transition from waking to not waking in response to the wake up message when: 9.54 V ≥ Power Supply 2 ≥ 6.8 V

NOTE: The thresholds observed in this test may not be the normal mode thresholds, but may be special sleep mode thresholds. The transceiver used in the Master should also be tested on its own or in a slave device to ensure compliance with this spec item.

7.4.1.6 Slave Node V_{il} Level Measurement and Input Threshold Hysteresis (V_{ih} - V_{il})

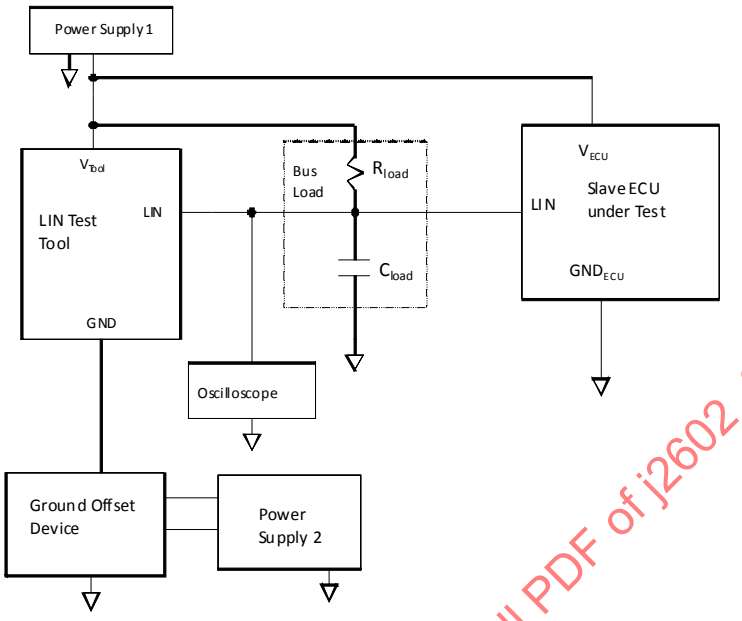

FIGURE 18 - SLAVE NODE V_{IL} LEVEL MEASUREMENT TEST SETUP

This test verifies the dominant input threshold of the Slave DUT is within the specified range under maximum and minimum supply voltages.

TABLE 43A - SLAVE NODE V_{IL} LEVEL MEASUREMENT TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.4.1.6.x (2 cases)
Parameter	V_{ECU} R_{load} C_{load}	See Table 43B Set to 875 Ω Set to 5.5 nF
Test Steps	For each entry in Table 43B: 1. Set Power Supply 2 to 0.2*V_{ECU} or adjust Ground Offset Device to obtain the desired voltage 2. LIN tool transmits a Targeted Reset to the DUT 3. LIN tool transmits a $3D header to the DUT 4. If the slave sends a response to the header go to step 5, if not go to step 6 5. Increase Power Supply 2 by 0.1 Volt or adjust Ground Offset Device to obtain the desired voltage and repeat step 2 6. Record the last Power Supply 2 setting where the Slave responded to the $3D header 7. Repeat steps 1 – 6 20 times 8. Calculate Input Threshold Hysteresis (V_{ih} - V_{il}) with average of values from section 7.4.1.4 and 7.4.1.6.	
Response	See Table 43B	
Reference	SAE J2602-1, 7.4.1	

TABLE 43B - SLAVE NODE V_{IL} LEVEL MEASUREMENT TEST PLAN

# Test	V_{ECU}	Response
7.4.1.6.1	8.0 V	The Slave must transition from responding to not responding to the $3D header when: 4.24 V ≥ Power Supply 2 ≥ 2.8 V
7.4.1.6.2	18.0 V	The Slave must transition from responding to not responding to the $3D header when: 9.54 V ≥ Power Supply 2 ≥ 6.8 V

7.4.1.7 Master Node $T_{r\text{-}d\ max}$ and $T_{d\text{-}r\ max}$ Measurement

This test verifies the recessive to dominant and dominant to recessive transition times of the Master DUT are within the specified range under maximum and minimum supply voltages.

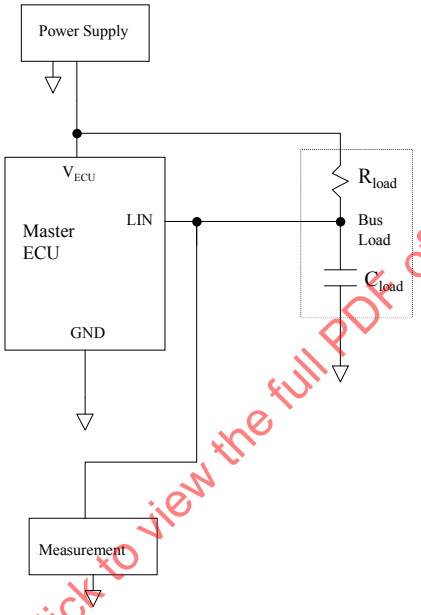

FIGURE 19 - MASTER NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST SETUP

TABLE 44A - MASTER NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST PLAN

DUT node as	Master ECU With C = 680pF	Test case 7.4.1.7.x (4 cases)
Parameter	V_{ECU} R_{load} and C_{load}	See Table 44B See Table 44B
Test Steps	For each entry in Table 44B: 1. Master Node transmits any message 2. D3 and D4 are measured during the synch byte. 3. Repeat steps 1-2 20 times.	
Response	See Table 44B	
Reference	SAE J2602-1, 7.4.1	

TABLE 44B - MASTER NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST PLAN

# Test	V_{ECU}	R_{load}	C_{load}	Response
7.4.1.7.1	8.0 V	4.0 kΩ	5.5 nF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.7.2	8.0 V	20 kΩ	889 pF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.7.3	18.0 V	4.0 kΩ	5.5 nF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.7.4	18.0 V	20 kΩ	889 pF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.

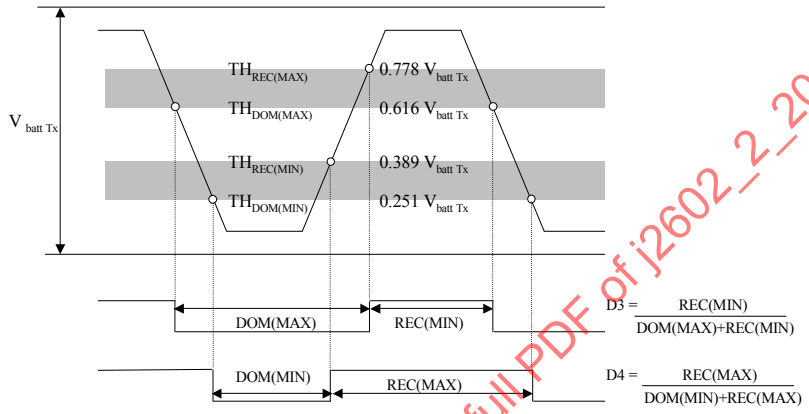

FIGURE 20 - $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT DESCRIPTION

7.4.1.8 Slave Node $T_{r\text{-}d\ max}$ and $T_{d\text{-}r\ max}$ Measurement

This test verifies the recessive to dominant and dominant to recessive transition times of the Slave DUT are within the specified range under maximum and minimum supply voltages.

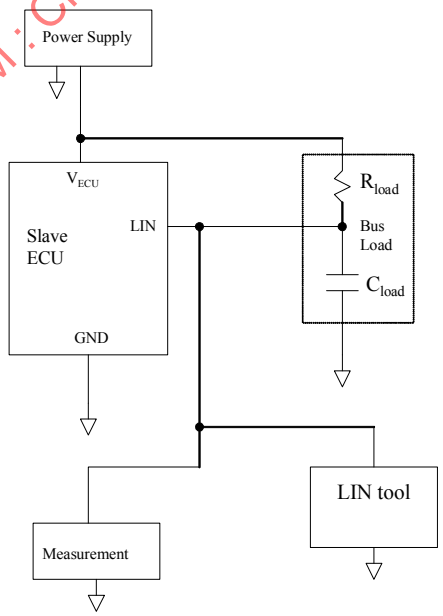

FIGURE 21 - SLAVE NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST SETUP

TABLE 45A - SLAVE NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.4.1.8.x (4 cases)
Parameter	V_{ECU} R_{load} and C_{load}	See Table 45B See Table 45B
Test Steps	1. LIN tool transmits a Targeted Reset to the DUT 2. LIN tool transmits a $3D header to the DUT 3. Measure D3 and D4 during the lower nibble of the RSID byte in the DUT response. 4. Repeat steps 1-3 20 times.	
Response	See Table 45B	
Reference	SAE J2602-1, 7.4.1	

TABLE 45B - SLAVE NODE $T_{R\text{-}D\ MAX}$ AND $T_{D\text{-}R\ MAX}$ MEASUREMENT TEST PLAN

# Test	V_{ECU}	R_{load}	C_{load}	Response
7.4.1.8.1	8.0 V	875 Ω	5.5 nF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.8.2	8.0 V	900 Ω	889 pF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.8.3	18.0 V	875 Ω	5.5 nF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.
7.4.1.8.4	18.0 V	900 Ω	889 pF	Measure D3 and D4 of the Synch Byte Field as shown in Figure 20. D3 ≥ 0.417, D4 ≤ 0.590.

7.4.1.9 Master Node Termination Resistance

This test verifies the load resistor in the Master DUT is within the specified range.

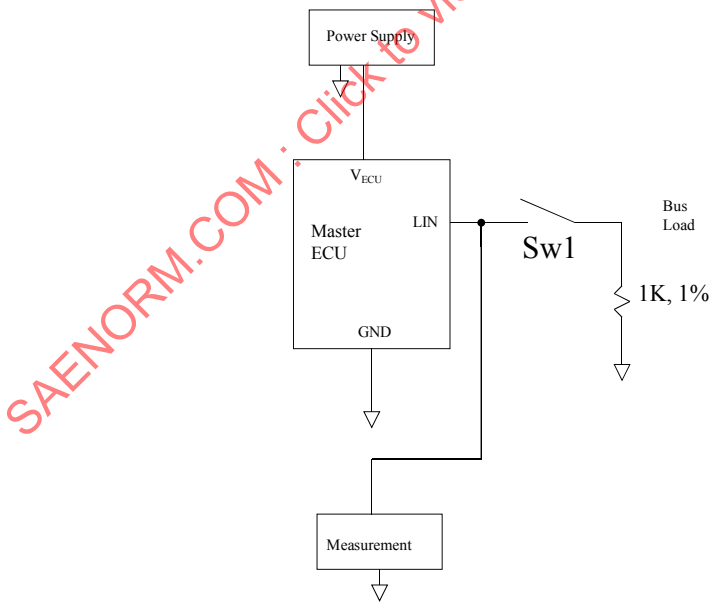

FIGURE 22 - MASTER NODE RESISTOR MEASUREMENT TEST SETUP

TABLE 46A - MASTER NODE RESISTOR MEASUREMENT TEST PLAN

DUT node as	Master ECU	Test case 7.6.1.1
Parameter	V_{ECU}	See Table 46B
Test Steps	1. Ensure the DUT is awake. Typically applying power will wake up the DUT. 2. Open Sw1. 3. The voltages specified in Table 46B are applied. 4. The voltage of the LIN bus is measured, V1. 5. Close Sw2. 6. The voltages specified in Table 46B are applied. 7. The voltage of the LIN bus is measured, V2. 8. R_{DUT} = 1K (V1/(V2 -1))	
Response	See Table 46B	
Reference	SAE J2602-1, 7.6.1.1 and 7.6.1.2	

TABLE 46B - MASTER NODE RESISTOR MEASUREMENT TEST PLAN

# Test	V_{ECU}	V_{ECU} Slew rate	Response
7.4.1.9.1	12.0V	N/A	900 <= R_{DUT} <= 1100

7.4.1.10 Slave Node Termination Resistance

This test verifies the load resistor in the Slave DUT is within the specified range.

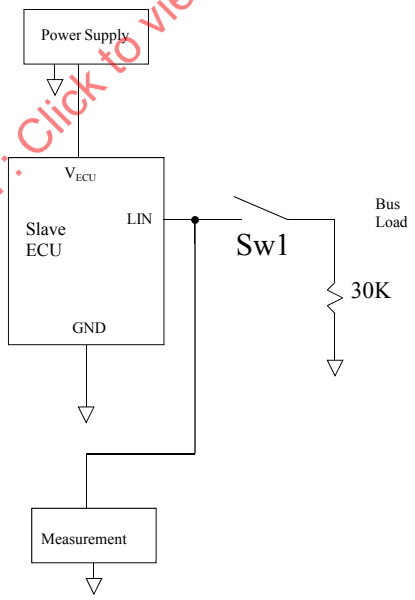

FIGURE 23 - SLAVE NODE RESISTOR MEASUREMENT TEST SETUP

TABLE 47A - SLAVE NODE RESISTOR MEASUREMENT TEST PLAN

DUT node as	Slave ECU	Test case 7.4.1.10
Parameter	V_{ECU}	See Table 47B
Test Steps	1. Ensure the DUT is awake. Typically applying power will wake up the DUT. 2. Open Sw1. 3. The voltages specified in Table are applied. 4. The voltage of the LIN bus is measured, V1. 5. Close Sw2. 6. The voltages specified in Table XXXX are applied. 7. The voltage of the LIN bus is measured, V2. 8. R_{DUT} = 30K (V1/(V2 -1))	
Response	See Table 47B	
Reference	SAE J2602-1, 7.4.1	

TABLE 47B - SLAVE NODE RESISTOR MEASUREMENT TEST PLAN

# Test	V_{ECU}	V_{ECU} Slew rate	Response
7.4.1.10.1	12.0V	N/A	20K <= R_{DUT} <= 60K

7.4.1.11 Master and Slave Node ECU Time Constant and Capacitance Measurement

This test measures the capacitance between the LIN pin and ground.

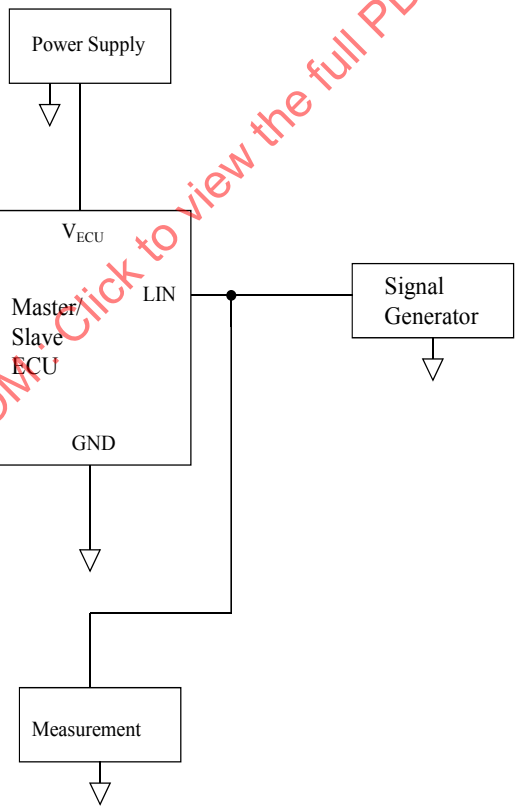

FIGURE 24 – MASTER OR SLAVE NODE CAPACITOR MEASUREMENT TEST SETUP

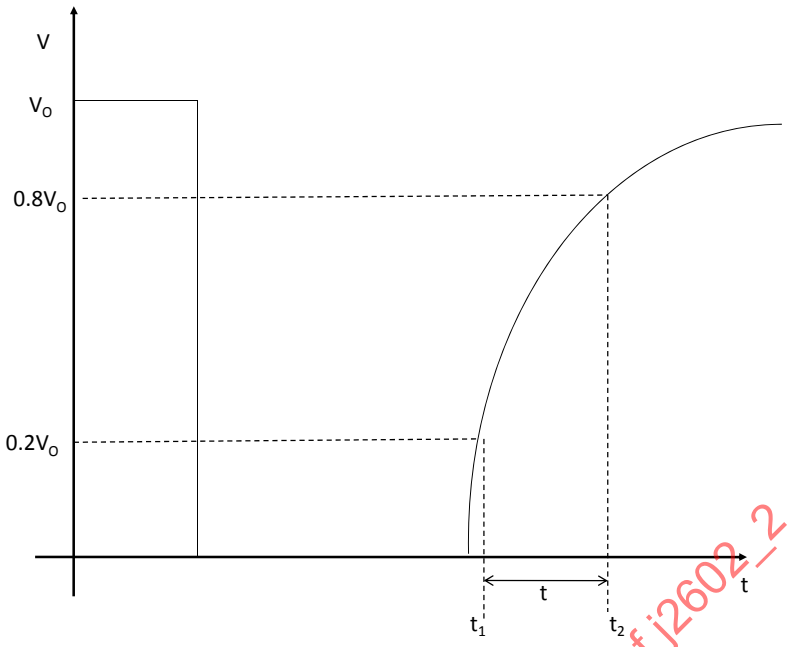

FIGURE 25 - MASTER OR SLAVE NODE NETWORK TIME CONSTANT MEASUREMENT

TABLE 48A - MASTER OR SLAVE NODE CAPACITANCECAPACITANCE MEASUREMENT TEST PLAN

DUT node as	Master ECU	Test case 7.4.1.11.1
DUT node as	Slave ECU	Test case 7.4.1.11.2
Parameter	V_{ECU}	See Table 48B
Test Steps	1. Ensure the DUT is asleep. 2. Apply a 12V, 100-us 0V pulse to the LIN pin with the signal generator. 3. Measure the rise time of the LIN bus according to Figure 25, τ = 0.721 (t2 - t1) 4. C = τ / R, where: R = Device resistance as measured in section 7.4.1.10..	
Response	See Table 48B	
Reference	SAE J2602-1, 7.4.1	

TABLE 48B - MASTER OR SLAVE NODE CAPACITANCE MEASUREMENT TEST PLAN

# Test	V_{ECU}	V_{ECU} Slew rate	Response
7.4.1.11.1	12.0V	N/A	90 <= C <=2450 pF.
7.4.1.11.2	12.0V	N/A	90 <= C <=270 pF.

7.5 Master / Slave LIN Data Link (UART) Requirements

Any device (e.g., UART, SCI, software, etc.) chosen to implement a J2602-1 LIN data link interface shall meet all requirements in this section.

7.5.1 Sample Point

This test verifies the Sample Point of the DUT is within the specified range by shifting a dominant to recessive edge until the message is no longer received properly.

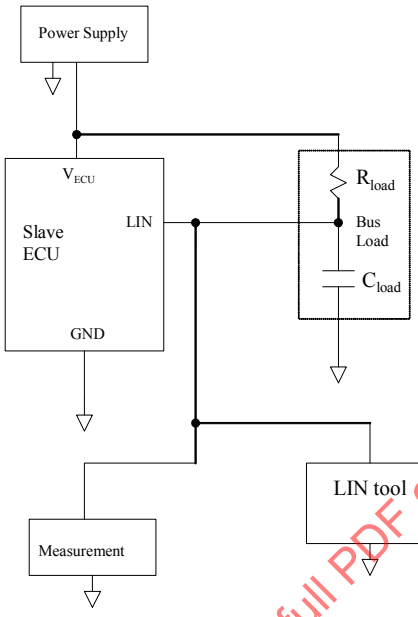

FIGURE 26 - SAMPLE POINT TEST SETUP

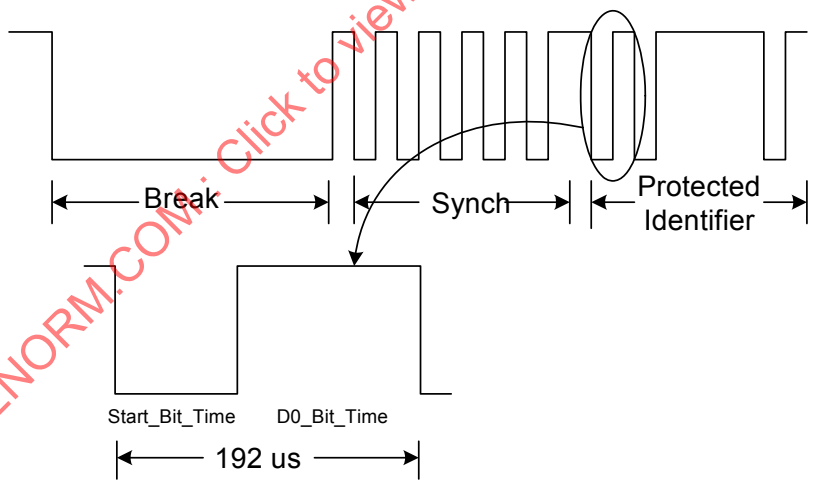

FIGURE 27 - DOMINANT TO RECESSIVE EDGE SHIFTING DESCRIPTION

7.5.1.1 Fixed Clock Slave Node

7.5.1.1.1 Max Bit Sample Timing Slave Node

TABLE 49A - MAX SAMPLE POINT - FIXED CLOCK SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.5.1.1.1.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 49B
Test Steps	1. Max_Sample_Point = 70.0 µsec 2. Start_Bit_Time = 70.0 µsec 3. D0_Bit_Time = 122.0 µsec 4. LIN tool transmits a Targeted Reset to the DUT 5. Start_Bit_Time = Start_Bit_Time – 1.0 µsec, D0_Bit_Time = D0_Bit_Time + 1.0 µsec, Max_Sample_Point = Start_Bit_Time 6. LIN tool transmits a $3D header to the DUT, using Start_Bit_Time and D0_Bit_Time values when sending $3D Protected Identifier ($7D). See Figure 2727. 7. If DUT responds to $3D header, then go to Step 4 8. Run test 20 times	
Response	See Table 49B	
Reference	SAE J2602-1, 7.5.1	

TABLE 49B - MAX SAMPLE POINT - FIXED CLOCK SLAVE TEST PLAN

# Test	R_{load}	C_{load}	Response
7.5.1.1.1.1	875 Ω	5.5 nF	Max_Sample_Point must be <= 63 µsec (10/16 bit times + 1.5%)
7.5.1.1.1.2	900 Ω	889 pF	Max_Sample_Point must be <= 63 µsec (10/16 bit times + 1.5%)

7.5.1.1.2 Min Bit Sample Timing Slave Node

TABLE 50A - MIN SAMPLE POINT - FIXED CLOCK SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.5.1.1.2.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 50B
Test Steps	1. Min_Sample_Point = 125.0 µsec 2. Start_Bit_Time = 125.0 µsec 3. D0_Bit_Time = 67.0 µsec 4. LIN tool transmits a Targeted Reset to the DUT 5. Start_Bit_Time = Start_Bit_Time + 1.0 µsec, D0_Bit_Time = D0_Bit_Time – 1.0 µsec, Min_Sample_Point = Start_Bit_Time 6. LIN tool transmits a $3D header to the DUT, using Start_Bit_Time and D0_Bit_Time values when sending $3D Protected Identifier ($7D). See Figure 27. 7. If DUT responds to $3D header, then go to Step 4 8. Run test 20 times	
Response	See Table 50B	
Reference	SAE J2602-1, 7.5.1	

TABLE 50B - MIN SAMPLE POINT - FIXED CLOCK SLAVE TEST PLAN

# Test	R_{load}	C_{load}	Response
7.5.1.1.2.1	875 Ω	5.5 nF	Min_Sample_Point must be >= 133 µsec (1 7/16 bit times - 1.5%)
7.5.1.1.2.2	900 Ω	889 pF	Min_Sample_Point must be >= 133 µsec (1 7/16 bit times - 1.5%)

7.5.1.2 Autobauding Slave Node

7.5.1.2.1 Max Bit Sample Timing Slave Node

TABLE 51A - MAX SAMPLE POINT - AUTOBAUDING CLOCK SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.5.1.2.1.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 51B
Test Steps	1. Max_Sample_Point = 70.0 µsec 2. Start_Bit_Time = 70.0 µsec 3. D0_Bit_Time = 122.0 µsec 4. LIN tool transmits a Targeted Reset to the DUT 5. Start_Bit_Time = Start_Bit_Time – 1.0 µsec, D0_Bit_Time = D0_Bit_Time + 1.0 µsec, Max_Sample_Point = Start_Bit_Time 6. LIN tool transmits a $3D header to the DUT, using Start_Bit_Time and D0_Bit_Time values when sending $3D Protected Identifier ($7D). See Figure 27. 7. If DUT responds to $3D header, then go to Step 4 8. Run test 20 times	
Response	See Table 51B	
Reference	SAE J2602-1, 7.5.1	

TABLE 51B - MAX SAMPLE POINT - AUTOBAUDING CLOCK SLAVE TEST PLAN

# Test	R_{load}	C_{load}	Response
7.5.1.2.1.1	875 Ω	5.5 nF	Max_Sample_Point must be <= 64 µsec (10/16 bit times + 2.0%)
7.5.1.2.1.2	900 Ω	889 pF	Max_Sample_Point must be <= 64 µsec (10/16 bit times + 2.0%)

7.5.1.2.2 Min Bit Sample Timing Slave Node

TABLE 52A - MIN SAMPLE POINT - AUTOBAUDING CLOCK SLAVE TEST PLAN

DUT node as	Slave ECU With C = 220pF	Test case 7.5.1.2.2.x (2 cases)
Parameter	V_{ECU} R_{load} and C_{load}	12V See Table 52B
Test Steps	1. Min_Sample_Point = 125.0 µsec 2. Start_Bit_Time = 125.0 µsec 3. D0_Bit_Time = 67.0 µsec 4. LIN tool transmits a Targeted Reset to the DUT 5. Start_Bit_Time = Start_Bit_Time + 1.0 µsec, D0_Bit_Time = D0_Bit_Time – 1.0 µsec, Min_Sample_Point = Start_Bit_Time 6. LIN tool transmits a $3D header to the DUT, using Start_Bit_Time and D0_Bit_Time values when sending $3D Protected Identifier ($7D). See Figure 27. 7. If DUT responds to $3D header, then go to Step 4 8. Run test 20 times	
Response	See Table 52B	
Reference	SAE J2602-1, 7.5.1	

TABLE 52B - MIN SAMPLE POINT - AUTOBAUDING CLOCK SLAVE TEST PLAN

# Test	R_{load}	C_{load}	Response
7.5.1.2.2.1	875 Ω	5.5 nF	Min_Sample_Point must be >= 133 µsec (1 7/16 bit times – 2.0%)
7.5.1.2.2.2	900 Ω	889 pF	Min_Sample_Point must be >= 133 µsec (1 7/16 bit times – 2.0%)