INTERNATIONAL STANDARD

ISO/IEC 7816-3

Second edition
1997-12-15

Information technology — Identification cards — Integrated circuit(s) cards with contacts —

Part 3:
Electronic signals and transmission protocols

Technologies de l'information — Cartes d'identification — Cartes à circuit(s) intégré(s) à contacts —

Partie 3: Signaux électroniques et protocoles de transmission

Reference number
ISO/IEC 7816-3:1997(E)

Contents

Page

Foreword iii
Introduction iv

1 Scope 1
2 Normative references 1
3 Terms and definitions 1
4 Electrical characteristics 2
4.1 General 2
4.2 Operating conditions 2
4.3 Voltage and current values 3
5 Card operating procedure 6
5.1 General overview 6
5.2 Activation 6
5.3 Information exchange 6
5.4 Deactivation 7
6 Answer-to-Reset 8
6.1 General configuration 8
6.2 Parameter T 8
6.3 Asynchronous character 9
6.4 Answer-to-Reset structure 10
6.5 Content of the global interface bytes 11
6.6 Modes of operation 13
7 Protocol and parameters selection 14
7.1 General 14
7.2 PPS protocol 14
7.3 Structure and content of PPS request and response 14
7.4 Successful PPS exchange 15
8 Protocol T=0, half-duplex transmission of asynchronous characters 15
8.1 Scope 15
8.2 Character level 15
8.3 Structure and processing of commands 15
9 Protocol T=1, half-duplex asynchronous transmission of blocks 17
9.1 Scope and principles 17
9.2 Terms and definitions 17
9.3 Character frame 18
9.4 Block frame 18
9.5 Protocol parameters 20
9.6 Character component operation at data link layer 21
9.7 Block component operation at data link layer 21

Annex A (informative) Scenarios for T=1 24

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 7816-3 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Identification cards and related devices*.

This second edition cancels and replaces the first edition (ISO/IEC 7816-3:1989), which has been technically revised. It also incorporates Amendment 1:1992 and Amendment 2:1994.

ISO/IEC 7816 consists of the following parts, under the general title *Information technology — Identification cards — Integrated circuit(s) cards with contacts*:

— *Part 1: Physical characteristics*

— *Part 2: Dimensions and location of the contacts*

— *Part 3: Electronic signals and transmission protocols*

— *Part 4: Interindustry commands for interchange*

— *Part 5: Numbering system and registration procedure for application identifiers*

— *Part 6: Interindustry data elements*

— *Part 7: Interindustry commands for structured card query language*

Annex A of this part of ISO/IEC 7816 is for information only.

Introduction

ISO/IEC 7816 is a series of International Standards describing the parameters for integrated circuit(s) cards with contacts and the use of such cards for international interchange.

The integrated circuit(s) cards with contacts are identification cards intended for information exchange negotiated between the outside and the integrated circuit within the card. During each information exchange, the card delivers information (computation results, stored data) and/or modifies its content (data storage, event memorization).

During the preparation of this International Standard, information was gathered concerning relevant patents upon which application of this standard might depend. Relevant patents were identified in France and USA, the patent holder being Bull S.A. in each case. However, ISO cannot give authoritative or comprehensive information about the evidence, validity or scope of the patents or similar rights.

The patent holder has stated that licenses will be granted in appropriate terms to enable the application of this part of ISO/IEC 7816, provided that those who seek licenses agree to reciprocate.

Further information is available from

BULL S.A.
BP 45
F 78430 Louveciennes
FRANCE

Information technology — Identification cards — Integrated circuit(s) cards with contacts —

Part 3:
Electronic signals and transmission protocols

1 Scope

This part of ISO/IEC 7816 specifies the power and signal structures, and information exchange between an integrated circuit(s) card and an interface device such as a terminal.

It also covers signal rates, voltage levels, current values, parity convention, operating procedure, transmission mechanisms and communication with the card.

It does not cover information and instruction content, such as identification of issuers and users, services and limits, security features, journaling and instruction definitions.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ISO/IEC 7816. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this part of ISO/IEC 7816 are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of ISO and IEC maintain registers of currently valid International Standards.

ISO 1177:1985, *Information processing — Character structure for start/stop and synchronous character oriented transmission.*

ISO/IEC 3309:1993, *Information technology — Telecommunications and information exchange between systems — High-level data link control (HDLC) procedures — Frame structure.*

ISO/IEC 7810:1995, *Identification cards — Physical characteristics.*

ISO 7816-1:1987[1)], *Identification cards — Integrated circuit(s) cards with contacts — Part 1: Physical characteristics.*

ISO 7816-2:1988[1)], *Identification cards — Integrated circuit(s) cards with contacts — Part 2: Dimensions and location of the contacts.*

ISO/IEC 7816-4:1995, *Information technology — Identification cards — Integrated circuit(s) cards with contacts — Part 4: Interindustry commands for interchange.*

1) Currently under revision.

3 Terms and definitions

The term "identification card" is defined in ISO/IEC 7810. For the purposes of this part of ISO/IEC 7816, the following definitions apply.

3.1 devices

3.1.1
interface device
terminal, communication device or machine to which the card is electrically connected during operation

3.1.2
operating card
card which can correctly carry out all its functions

3.2
etu (abbreviation for "elementary time unit")
nominal duration of a moment on contact I/O

3.3 resets

3.3.1
cold reset
first reset occurring after activation

3.3.2
warm reset
any reset which is not a cold reset

For the purposes of this part of ISO/IEC 7816, the following notations apply.

state H high state logic level

state L low state logic level

state Z mark or high state, as defined in ISO 1177

state A space or low state, as defined in ISO 1177

'XY' hexadecimal notation, equal to XY to the base 16

4 Electrical characteristics

4.1 General

4.1.1 Electrical circuits

Contact assignments are specified in ISO 7816-2, supporting at least the following electrical circuits.

GND ground, reference voltage

VCC power supply input

I/O input or output for serial data

CLK clock signal input

RST reset signal input

VPP programming power input, optional use by the card

4.1.2 Abbreviations

For the purposes of this clause, the following abbreviations apply.

C_{IN} input capacitance

C_{OUT} output capacitance

I_{CC} current at VCC

I_{IH} high level input current

I_{IL} low level input current

I_{OH} high level output current

I_{OL} low level output current

I_{PP} current at VPP

t_F fall time, from 90 % to 10 % of signal amplitude

t_R rise time, from 10 % to 90 % of signal amplitude

V_{CC} voltage at VCC

V_{IH} high level input voltage

V_{IL} low level input voltage

V_{OH} high level output voltage

V_{OL} low level output voltage

V_{PP} voltage at VPP

4.2 Operating conditions

4.2.1 Classes of operating conditions

This part of ISO/IEC 7816 defines two classes of operating conditions. Through contact VCC, the interface device shall provide to the card the following nominal supply voltage:

- 5 V under class A,
- 3 V under class B.

Consequently, cards and interface devices shall work either in class A only, or in class B only, or in class A and in class B, denoted as class AB later on.

Class A cards shall operate with class A and class AB interface devices. Class AB cards shall operate with class A, class B and class AB interface devices. Class B cards shall operate with class B and class AB interface devices; they shall be designed in such a way that they will not be damaged under class A operating conditions (by definition, a damaged card no longer operates as specified or contains corrupt data).

4.2.2 Selection of the operating class

Figure 1 shows the decisions to be made by an interface device in selecting the class of operating conditions to be applied to a card. Decisions shown are based upon information implicit in the interface device, except where the word "card" is present.

When available in the interface device, the first operating conditions to be applied to the card shall be class B.

Under class A operating conditions, a class B card shall not provide an Answer-to-Reset (see 6).

If the card does not provide an Answer-to-Reset, then the interface device shall deactivate the card; after a delay of at least 10 ms, the interface device shall apply the operating conditions of the next available class.

If the card provides an Answer-to-Reset without a class indicator (see 6.5.6), then the interface device shall apply or maintain class A operating conditions when available, or deactivate the card.

If the card provides an Answer-to-Reset with a class indicator, and the interface device is applying a class of operating conditions supported by the card, then normal operation may continue.

If the Answer-to-Reset does not indicate the current class of operating conditions, but another class supported by the interface device, then the interface device shall deactivate the card; after a delay of at least 10 ms, the interface device shall apply the operating conditions of that class.

NOTE — Some cards conforming to ISO/IEC 7816-3:1989 could be damaged when operating under class B conditions and should be used only in class A interface devices.

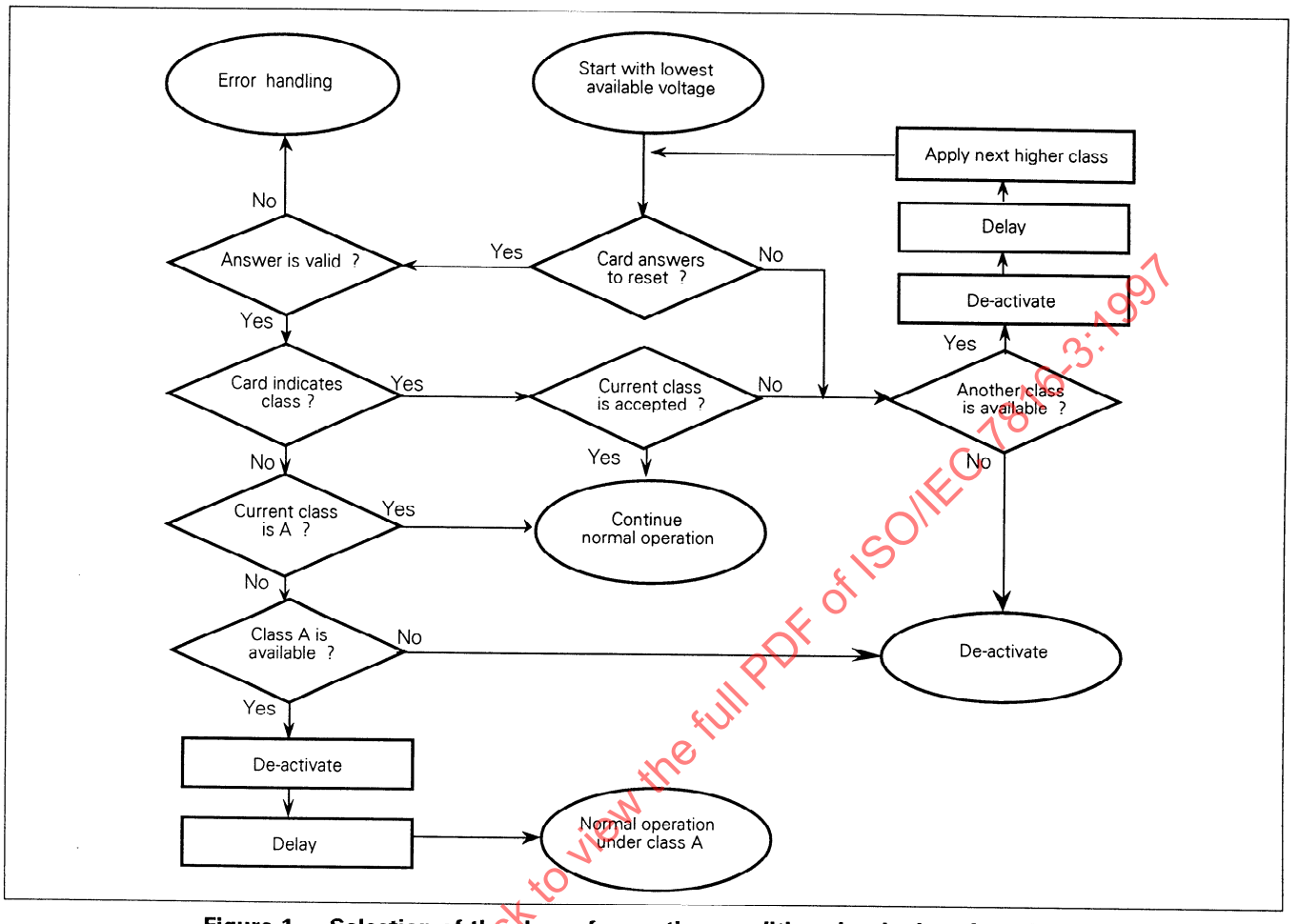

Figure 1 — Selection of the class of operating conditions by the interface device

4.3 Voltage and current values

4.3.1 Measurement conventions

All measurements are defined with respect to contact GND and in an ambient temperature range from 0° C to 50° C. All currents flowing into the card are considered positive. All timings shall be measured with respect to the appropriate threshold levels as defined in 4.3.2 to 4.3.6.

An electrical circuit is not active when the voltage with respect to contact GND remains between 0 V and 0,4 V for currents less than 1 mA flowing into the interface device.

4.3.2 VCC

This contact is used to provide the card with the power supply. In table 1, the current value is averaged over 1 ms. The maximum current is defined for the card. The interface device shall be able to deliver this current within the range specified for the voltage values and may deliver more.

Table 1 — Electrical characteristics of VCC under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{CC}	Class A Class B	4,5 2,7	5,5 3,3	V
I_{CC}	Class A, at maximum allowed frequency Class B, at maximum allowed frequency When the clock is stopped (see 5.3.4)		60 50 0,5	mA

The power supply shall maintain the voltage value in the specified range despite transient power consumption as defined in table 2.

Table 2 — Spikes on I_{CC}

Class	Maximum charge [a]	Maximum duration	Maximum variation [b] of I_{cc}
A	20 nA.s	400 ns	100 mA
B	10 nA.s	400 ns	50 mA

[a] The maximum charge is half the product of the maximum duration and the maximum variation.
[b] The maximum variation is the difference in supply current with respect to the average value.

4.3.3 I/O

This contact is used as input (reception mode) or output (transmission mode). The information exchange through contact I/O uses the following two logic states as defined in ISO 1177:

— state Z if the card and the interface device are in reception mode or if this state is imposed by the transmitter;

— state A if this state is imposed by the transmitter.

When the two ends of the line are in reception mode, the line shall be at state Z (high state). When the two ends are in non-matched transmit mode, the logic state of the line may be indeterminate. During operation, the interface device and the card shall not both be in transmit mode.

The interface device shall be able to support the defined range of input currents when the input voltages are in the allowed range. The interface device shall present to the card an impedance such that it will not prevent the card from being able to keep the output voltages in the defined range.

Table 3 — Electrical characteristics of I/O under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{IH} I_{IH}	 V_{IH}	0,70 x V_{CC} −300	V_{CC} +20	V µA
V_{IL} I_{IL}	 V_{IL}	0 −1000	0,15 x V_{CC} +20	V µA
V_{OH} I_{OH}	External pull-up resistor: 20 kΩ to V_{CC} V_{OH}	0,70 x V_{CC}	V_{CC} +20	V µA
V_{OL}	I_{OL} = 1 mA [a]	0	0,15 x V_{CC}	V
t_R t_F	C_{IN} = 30 pF; C_{OUT} = 30 pF		1	µs

The voltage on I/O shall remain between −0,3 V and V_{CC} + 0,3 V.

[a] Interface device implementations should not require the card to sink more than 500 µA.

4.3.4 CLK

This contact is used to provide the card with the clock signal. The actual value of the frequency of the clock signal is designated by *f*. See 5.2 and 6.5.2 for the ranges of values of *f*.

The duty cycle of the clock signal shall be between 40 % and 60 % of the period during stable operation. When switching the frequency from one value to another, care should be taken to ensure that no pulse is shorter than 40 % of the shortest period allowed by the card as defined in table 7. No information shall be exchanged when switching the frequency value. Two different times are recommended for switching the frequency value:

— immediately after the answer to reset, or

— immediately after a successful PPS exchange (see 7.4).

Table 4 — Electrical characteristics of CLK under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{IH} I_{IH}	V_{IH}	0,70 x V_{CC} −20	V_{CC} +100	V µA
V_{IL} I_{IL}	V_{IL}	0 −100	0,5 +20	V µA
t_R t_F	C_{IN} = 30 pF		9 % of period	
The voltage on CLK shall remain between − 0,3 V and V_{CC} + 0,3 V.				

4.3.5 RST

This contact is used to provide the card with the reset signal according to either 5.3.2 (cold reset) or 5.3.3 (warm reset).

Table 5 — Electrical characteristics of RST under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{IH} I_{IH}	V_{IH}	0,80 x V_{CC} −20	V_{CC} +150	V µA
V_{IL} I_{IL}	V_{IL}	0 −200	0,12 x V_{CC} +20	V µA
t_R t_F	C_{IN} = 30 pF		1	µs
The voltage on RST shall remain between − 0,3 V and V_{CC} + 0,3 V.				

4.3.6 VPP

Under class B operating conditions, this contact is reserved for future use.

Under class A operating conditions, this contact may be used to provide the card with the programming power required to write or to erase the internal non-volatile memory. Table 6 defines two activated states on contact VPP: pause state and programming state. The interface device shall maintain contact VPP at pause state unless the card requires the programming state.

Table 6 — Electrical characteristics of VPP under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{PP} I_{PP}	Pause state	0,95 x V_{CC}	1,05 x V_{CC} 20	V mA
V_{PP} I_{PP}	Programming state	0,975 x P	1,025 x P I	V mA
t_R t_F		[a]	200	µs
The power shall not exceed 1,5 W when averaged over any period of 1 s. NOTES 1 When needed, the card provides the interface device with the values P and I (see 6.5.4). 2 VPP state control, as specified in clauses 8 and 9, is only relevant under class A operating conditions.				
[a] The rate of change of the voltage on VPP value shall not exceed 2 V.µs^{-1}.				

5 Card operating procedure

5.1 General overview

The electrical circuits shall not be activated until the contacts of the card are mechanically connected to the contacts of the interface device.

The interaction between the interface device and the card shall be conducted through the following consecutive operations specified in the subsequent subclauses.

— Activation of the electrical circuits by the interface device.

— Information exchange between the card and the interface device always initiated by the card answering to the cold reset.

— Deactivation of the electrical circuits by the interface device.

The sequence of deactivation of the electrical circuits should be concluded before the mechanical disconnection between the contacts of the card and the contacts of the interface device.

5.2 Activation

In order to initiate an interaction with a mechanically connected card, the interface device shall activate the electrical circuits in the following order shown on figure 2.

— RST shall be put to state L (see 4.3.5).

— VCC shall be powered according to the operating conditions selected by the interface device: class A or class B (see 4.3.2 and table 1).

— I/O in the interface device shall be put in reception mode (see 4.3.3).

— Under class A, VPP shall be put to pause state (see 4.3.6). Under class B, VPP is reserved for future use.

— CLK shall be provided with a clock signal (see 4.3.4). At least during the answer to reset, the frequency f of the clock signal shall lie in the range:

- 1 to 5 MHz under class A or
- 1 to 4 MHz under class B.

By the end of the sequence of activation of the electrical circuits (RST in state L, VCC powered, I/O in reception mode in the interface device, VPP at pause state when operating under class A, CLK provided with a suitable and stable clock signal), the card is ready for a cold reset according to the timing specified in 5.3.2 and figure 2.

5.3 Information exchange

5.3.1 General

If the card supports the class of operating conditions, then the card shall answer to any reset according to clause 6. After completion of any answer to reset, the interface device may initiate a warm reset of the card. The answer to a warm reset may differ from the answer to the previous, either cold or warm, reset. After completion of any answer to reset indicating the negotiable mode (see 6.6), the interface device may initiate a PPS exchange as specified in clause 7.

The operating procedure of commands depends on the transmission protocol. The half-duplex transmission of asynchronous characters with the interface device as the master is specified in clause 8. The half-duplex asynchronous transmission of blocks is specified in clause 9. When no transmission is expected from the card (e.g., after completion of a command and before initiating the next command), the interface device may even stop the clock signal if the card supports clock stop.

NOTE — ISO/IEC 7816-4 specifies interindustry commands for interchange. Other commands are specified either in existing standards or in additional standards to be defined.

5.3.2 Cold reset

According to figure 2, the clock signal is applied to CLK at time *Ta*. The card shall set the I/O line to state Z within 200 clock cycles of the clock signal (*ta*) being applied to CLK (time *ta* after *Ta*). The card is reset by maintaining RST at state L for at least 400 clock cycles (*tb*) after the clock signal is applied to CLK (time *tb* after *Ta*).

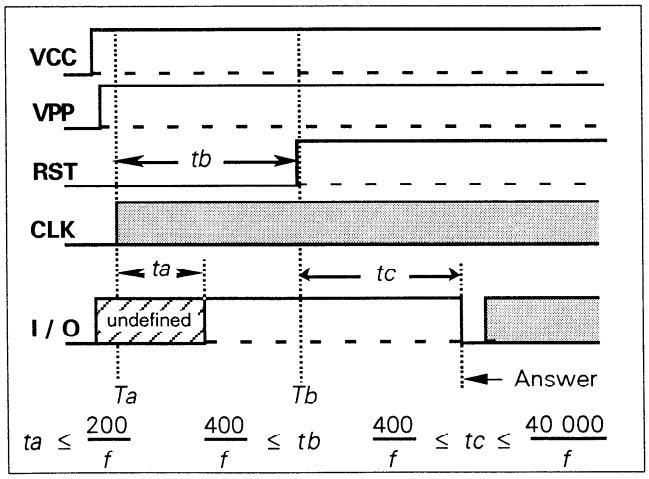

Figure 2 — Activation and cold reset

At time *Tb*, RST is put to state H. The answer on I/O shall begin between 400 and 40 000 clock cycles (*tc*) after the rising edge of the signal on RST (time *tc* after *Tb*).

If the answer does not begin within 40 000 clock cycles with RST at state H, the signal on RST shall be returned to state L and the electrical circuits shall be deactivated by the interface device according to 5.4.

NOTES

1 The internal state of the card is assumed not to be defined before a cold reset. Therefore the design of the card has to avoid improper operation.

2 The interface device may initiate a cold reset of the card at its discretion at any time.

5.3.3 Warm reset

According to figure 3, the interface device initiates a warm reset by putting RST to state L for at least 400 clock cycles (time *te*) while VCC and CLK remain stable.

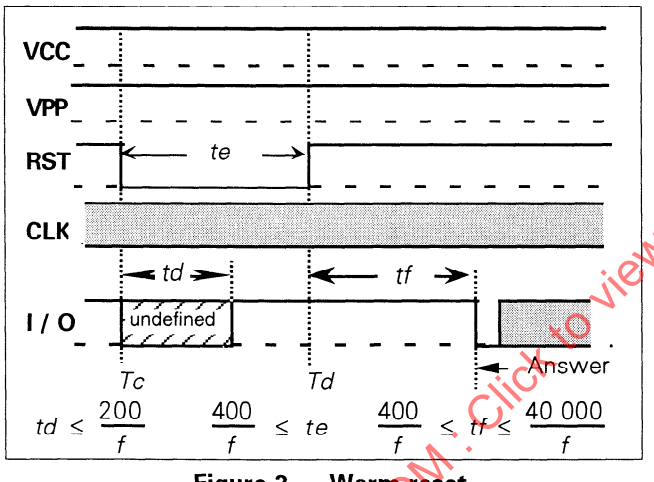

Figure 3 — Warm reset

At time *Td*, RST is put to state H. The answer on I/O shall begin between 400 and 40 000 clock cycles (*tf*) after the rising edge of the signal on RST (time *tf* after *Td*).

If the answer does not begin within 40 000 clock cycles with RST at state H, the signal on RST shall be returned to state L and the electrical circuits shall be deactivated by the interface device according to 5.4.

5.3.4 Clock stop

For cards supporting clock stop, when the interface device expects no transmission from the card and when I/O has remained at state Z for at least 1 860 clock cycles (time *tg*), then according to figure 4, the interface device may stop the clock on CLK (at time *Te*).

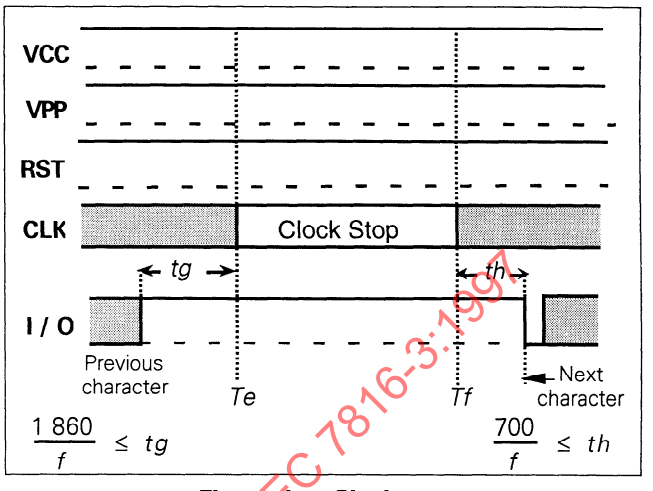

Figure 4 — Clock stop

When the clock is stopped (from time *Te* to time *Tf*), CLK shall be maintained either at state H or at state L; the state is indicated by parameter X as defined in 6.5.5.

At time *Tf*, the interface device restarts the clock and the information exchange on I/O may continue after at least 700 clock cycles (time *th* after *Tf*).

5.4 Deactivation

When information exchange is concluded or aborted (e.g., unresponsive card, detection of card removal), the interface device shall deactivate the electrical circuits in the following order shown on figure 5.

— RST shall be put to state L.

— CLK shall be put to state L (unless the clock is already stopped at state L).

— VPP shall be deactivated (if it has been activated).

— I/O shall be put to state A.

— VCC shall be deactivated.

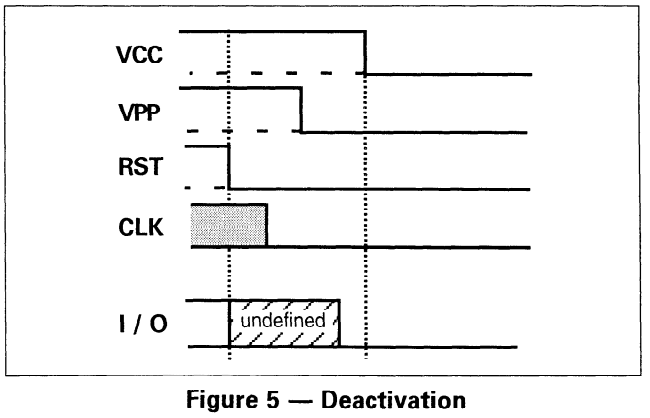

Figure 5 — Deactivation

6 Answer-to-Reset

6.1 General configuration

By definition, the Answer-to-Reset is the value of the sequence of bytes sent by the card to the interface device as the answer to a reset. On the I/O circuit, each byte is conveyed in an asynchronous character.

Each successful reset operation shall induce on I/O an initial character TS followed by at most 32 characters in the following order shown on figure 6.

T0 ..... Format character, mandatory

TA(i) TB(i) TC(i) TD(i) ..... Interface characters, optional

T1 T2 ...TK ..... Historical characters, optional

TCK ..... Check character, conditional

- The initial character sets up the convention to decode every subsequent character.
- The format character announces the first interface characters and all the historical characters.
- The presence of interface characters is indicated by a bit map technique initiated by the format character.
- The presence of historical characters is indicated by a number coded in the format character.
- The presence of the check character depends on the value(s) of parameter T in some interface bytes.

For notation simplicity, T0 TA(i) ... T1 ... TCK hereafter designate the bytes as well as the characters in which they are conveyed.

6.2 Parameter T

Parameter T refers to a transmission protocol and/or qualifies interface bytes. In every byte TD(i) (see 6.4.3.1), TA(2) (see 6.5.7) or PPS0 (see 7.3), the bits b4 to b1 code a value of parameter T.

— T=0 refers to the half-duplex transmission of asynchronous characters specified in clause 8.

— T=1 refers to the half-duplex asynchronous transmission of blocks specified in clause 9.

— T=2 and T=3 are reserved for future full-duplex operations.

— T=4 is reserved for an enhanced half-duplex transmission of asynchronous characters.

— T=5 to T=13 are reserved for future use.

— T=14 refers to transmission protocols not standardized by ISO/IEC JTC 1 SC 17.

— T=15 does not refer to a transmission protocol, but only qualifies global interface bytes (see 6.4.3.2).

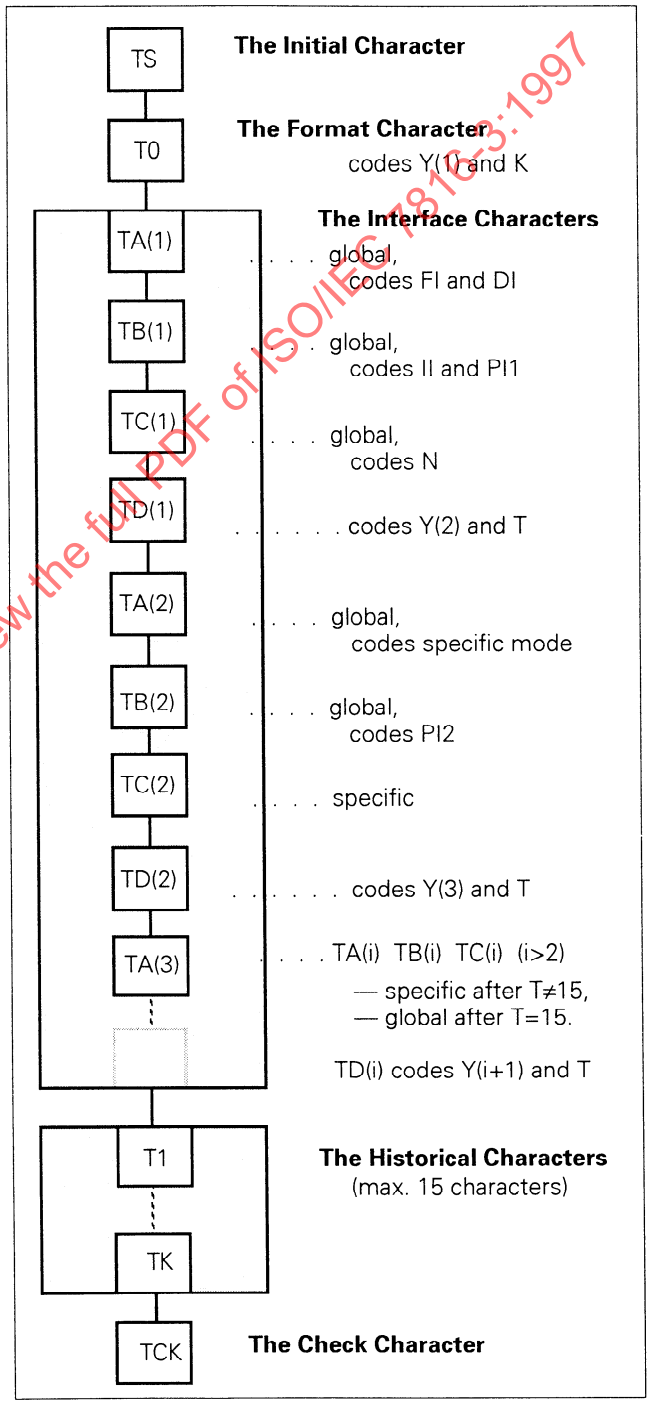

Figure 6 — Configuration of the Answer-to-Reset

6.3 Asynchronous character

6.3.1 Elementary time unit

During the answer to reset, the etu shall be equal to 372 clock cycles.

$$1 \text{ etu} = \frac{372}{f}$$

See also 6.4.1 for an alternate measurement of the etu value and 6.5.2 for its general expression.

6.3.2 Character frame

Before a character, the circuit I/O shall be at state Z. According to figure 7, a character consists of ten consecutive moments; each moment is either at state Z or at state A.

— The first moment m1 shall be at state A; this moment is the "start moment".

— The eight moments m2 to m9 convey a byte.

— The last moment m10 shall ensure the character parity; it conveys the "parity bit".

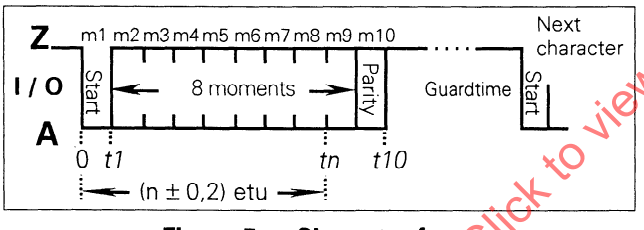

Figure 7 — Character frame

Within every character, if the state changes at the end of moment mn, then the delay from the character leading edge to the mn trailing edge shall be the following (see figure 7).

$$tn = (n \pm 0{,}2) \text{ etu}$$

The transmitter time origin is the character leading edge. When searching for a character, the receiver samples I/O periodically: the sampling time shall be less than 0,2 etu. The receiver time origin is the mean between the last observation of state Z and the first observation of state A.

The receiver shall confirm m1 before 0,7 etu (in receiver time). Then the receiver shall receive m2 at (1,5±0,2) etu, m3 at (2,5±0,2) etu, ... m9 at (8,5±0,2) etu and m10 at (9,5±0,2) etu. Character parity is checked on the fly.

NOTE — Such tolerances ensure that the signal measurement zones are all distinct from the signal transition zones.

The delay between the leading edges of two consecutive characters shall be at least 12 etu, i.e., the duration of one character, (10±0,2) etu, followed by a guardtime. While in guardtime, the card and the interface device shall remain both in reception mode (in error-free operation), so that I/O is maintained at state Z.

During the answer to reset, the delay between the leading edges of two consecutive characters sent by the card shall not exceed 9 600 etu. This maximum value is named "initial waiting time".

6.3.3 Error signal and character repetition

During the answer to reset, the following procedure is mandatory for the cards offering the protocol T=0; it is optional for the interface devices and for other cards.

As shown in figure 8, when character parity is incorrect, the receiver shall transmit an error signal by putting the I/O circuit to sate A at (10,5±0,2) etu in receiver time for one etu minimum, two etu maximum. Then the receiver shall expect a repetition of the character.

For detecting an error signal, the transmitter shall check the state of the I/O circuit at (11±0,2) etu in transmitter time, i.e., after the character leading edge.

— The correct reception is assumed if the state is Z.

— The incorrect reception is assumed if the state is A. After a delay of at least two etu after detection of the error signal, the transmitter shall repeat the character.

If no character repetition is provided by the card,

— the card ignores and shall not suffer damage from the error signal coming from the interface device;

— the interface device shall be able to initiate the repetition of the entire reset operation.

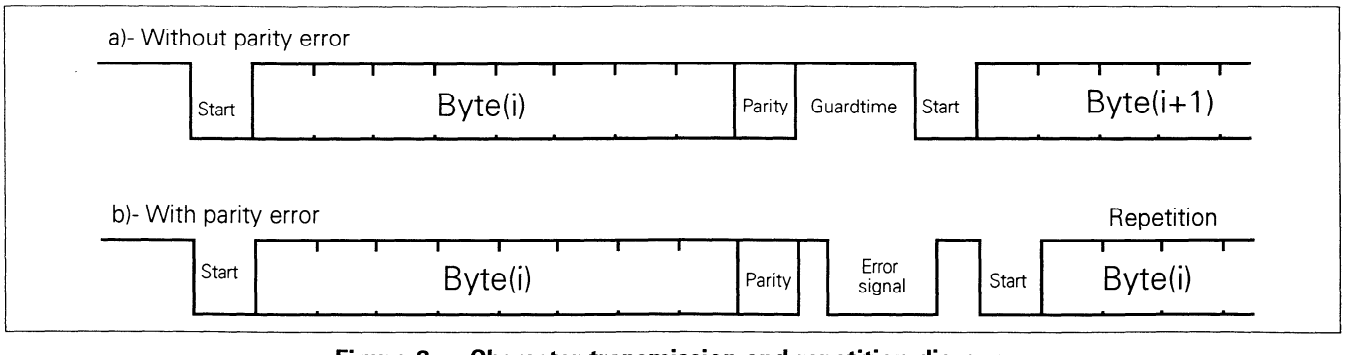

Figure 8 — Character transmission and repetition diagram

6.4 Answer-to-Reset structure

6.4.1 Initial character and coding convention

Figure 9 shows the initial character TS.

— The moments m1 to m4 define a synchronization sequence with value of (Z)AZZA.

— The moments m5 to m7 indicate inverse or direct convention with values of AAA or ZZZ respectively.

— The moments m8 to m10 are equal to AAZ.

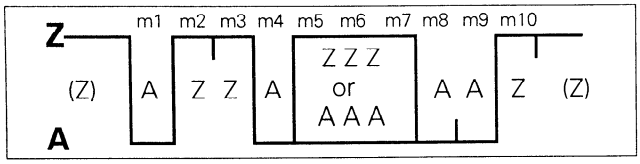

Figure 9 — Initial character TS

NOTE — The synchronization sequence allows the interface device to determine the etu initially used by the card. An alternate measurement of etu is a third of the delay between the first two falling edges in TS. Transmission and reception mechanisms in the card (including the tolerances described in 6.3.2 and 6.3.3) should be consistent with this alternate definition of etu.

TS sets up the convention to code bytes in all subsequent characters. The convention consists of

— the coding of values 1 and 0 by states Z and A for the nine moments m2 to m10,

— the bit significance for the eight moments m2 to m9.

Character parity is correct when there is an even number of bits set at 1 in the nine moments m2 to m10.

TS has two possible values shown as characters of ten moments at states Z or A and according to the coding convention, as bytes of eight bits with values of 1 or 0.

— Character (Z)AZZAAAAAAZ sets up the inverse convention where state A codes value 1 and moment m2 conveys the most significant bit (msb first). When decoded by inverse convention, the conveyed byte is equal to '3F'.

— Character (Z)AZZAZZZAAZ sets up the direct convention where state Z codes value 1 and moment m2 conveys the least significant bit (lsb first). When decoded by direct convention, the conveyed byte is equal to '3B'.

Figure 10 shows the byte frame as used hereafter. The byte consists of eight bits denoted as b8 to b1 with values of 1 or 0; b8 is the most significant bit (msb) and b1 the least significant bit (lsb).

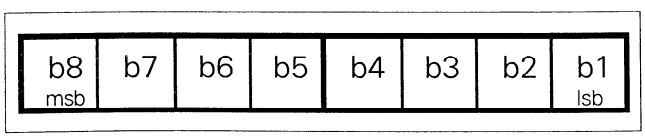

Figure 10 — Byte frame

6.4.2 Format byte T0

According to figure 11, byte T0 contains two parts.

— The bits b8 to b5 form Y(1); each bit equal to 1 indicates the presence of a further interface byte.

— The bits b4 to b1 form K which codes the number of historical bytes from 0 to 15.

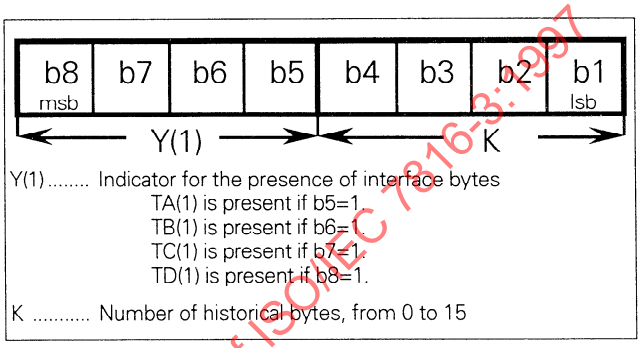

Figure 11 — Coding of T0

6.4.3 Interface bytes TA(i) TB(i) TC(i) TD(i)

6.4.3.1 TD(i)

According to figure 12, byte TD(i) contains two parts.

— The bits b8 to b5 form Y(i+1); each bit equal to 1 indicates the presence of a further interface byte.

— The bits b4 to b1 form a value of parameter T as defined in 6.2.

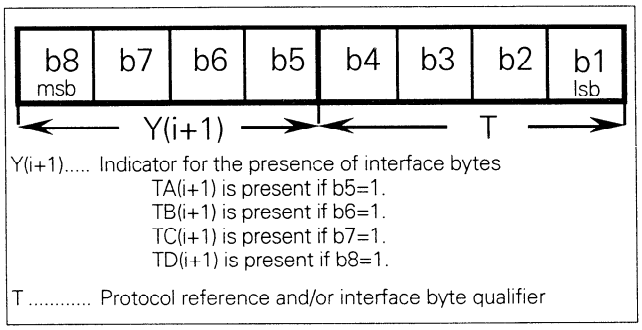

Figure 12 — Coding of TD(i)

Therefore T0 conveys Y(1) and TD(i) conveys Y(i+1). In the byte conveying Y(i), the bits b8 to b5 state whether byte TA(i) for b5, byte TB(i) for b6, byte TC(i) for b7, byte TD(i) for b8 are present or absent (depending on whether the relevant bit is equal to 1 or 0) in this order after the byte conveying Y(i).

If TD(i) is absent, the interface bytes TA(i+1), TB(i+1), TC(i+1) and TD(i+1) are absent.

If two or more values of parameter T are present in TD(1) TD(2) ..., they shall be present in ascending numerical order. If present, T=0 shall be first, T=15 shall be last. The value T=15 is forbidden in TD(1).

The "first offered protocol" is defined as follows.

— If TD(1) is present, then the first offer is T.

— If TD(1) is absent, then the only offer is T=0.

6.4.3.2 TA(i) TB(i) TC(i)

The interface bytes TA(i), TB(i) and TC(i) for i = 1, 2, 3, ... are either global or specific.

— Global interface bytes refer to parameters of the integrated circuit(s) within the card, see 6.5.

— Specific interface bytes refer to parameters of a transmission protocol offered by the card.

The interface bytes TA(1) TB(1) TC(1) TA(2) TB(2) are global. The interface byte TC(2) is specific; it is defined for T=0, see 8.2. The interpretation of the interface bytes TA(i) TB(i) TC(i) for i > 2 depends on the value of parameter T in TD(i–1).

— If T≠15, the bytes are protocol T specific.

— If T=15, the bytes are global.

If more than three interface bytes TA(i) TB(i) TC(i) are defined for the same value of parameter T and are present in the Answer-to-Reset, they shall be present subsequently after TD(i–1) TD(i) ... which all indicate the same value T; therefore, they are unambiguously identified as appearing after the first, the second or the nth occurrence of T in TD(i–1) for i > 2.

NOTE — The combination of parameter T with the bit map technique allows to send only useful interface bytes and when needed, to use default values for parameters corresponding to absent interface bytes.

6.4.4 Historical bytes T1 T2 ... TK

The historical bytes designate general information, for example, the card manufacturer, the chip inserted in the card, the masked ROM in the chip, the state of the life of the card. ISO/IEC 7816-4 specifies the content of the historical bytes.

If K is not null, then the Answer-to-Reset continues on K historical bytes T1 T2 ... TK.

6.4.5 Check byte TCK

The value of byte TCK shall be such that the exclusive-oring of all the bytes T0 to TCK inclusive is null.

If only T=0 is indicated, possibly by default, byte TCK shall be absent. If T=0 and T=15 are present and in all the other cases, byte TCK shall be present.

6.5 Content of the global interface bytes

6.5.1 General

This subclause specifies the content of the global interface bytes. ISO/IEC JTC 1 SC 17 reserves for future use all the global interface bytes not defined in this subclause and all the unused values of the integers defined hereafter in this subclause.

This subclause specifies the bytes TA(1) TB(1) TC(1) TA(2) TB(2) and TA(i) for i > 2 after the first occurrence of T=15 in TD(i–1). These bytes code in binary the unsigned positive integers FI, DI, II, PI1, N, PI2, XI and UI which are either equal to or used to compute the values of parameters F, D, N, P, I, X and U presented hereafter.

— If present, such a byte shall be interpreted in order to process correctly any protocol.

— If such a byte is absent, then when needed, default values shall be used for the relevant parameters.

TA(1) codes (see 6.5.2)

— FI, the reference to a clock rate conversion factor over the bits b8 to b5, see table 7.

— DI, the reference to a baud rate adjustment factor over the bits b4 to b1, see table 8.

TB(1) where b8 = 0 codes (see 6.5.4)

— II, the reference to the maximum programming current over the bits b7 b6, see table 9.

— PI1, the value of the programming voltage over the bits b5 to b1.

NOTE — The interface device may ignore the bit b8 of TB(1).

TC(1) codes (see 6.5.3)

— N, the reference to compute the extra guardtime over the eight bits.

TA(2) is the specific mode byte (see 6.5.7 and 6.6).

TB(2) codes (see 6.5.4) an alternative to PI1 using

— PI2, the value of the programming voltage over the eight bits.

TA(i) after the first occurrence of T=15 in TD(i–1) for i > 2 codes (see 6.5.5 and 6.5.6)

— XI, the reference to the clock stop indicator over the bits b8 b7, see table 10.

— UI, the reference to the class indicator over the bits b6 to b1, see table 11.

NOTE — Interface devices complying to ISO/IEC 7816-3:1989 normally ignore TA(i) TB(i) TC(i) after T=15 in TD(i–1) for i > 2 as interface bytes specific of a protocol they do not support.

6.5.2 Transmission factors F and D

Parameters F and D are respectively the clock rate conversion factor and the baud rate adjustment factor. The etu used on circuit I/O depends upon the actual values of transmission factors F and D. The etu shall be equal to F/D clock cycles.

$$1 \text{ etu} = \frac{F}{D} \times \frac{1}{f}$$

The minimum value of the frequency f shall be 1 MHz. The maximum value is given by table 7 as a function of FI. The default maximum value is 5 MHz.

For computing the etu, the pair of factors F and D shall take one of the following three pairs of values:

— Fi and Di, the values indicated by the card in TA(1) according to tables 7 and 8; if TA(1) is absent, then Fi and Di are set at default values;

— Fd and Dd, the default values 372 and 1;

— Fn and Dn, the values negotiated by a successful PPS exchange in the ranges Fd to Fi and Dd to Di.

During the answer to reset, Fd and Dd shall apply. After the answer to reset, the values of F and D depend upon the mode of operation (see 6.6).

— In the negotiable mode (see 6.6.3), Fd and Dd shall continue to apply until a PPS exchange has been successfully completed (see 7.4). Immediately after the successful PPS exchange, Fn and Dn shall apply.

— In the specific mode (see 6.6.2),

- if b5=0 in TA(2), Fi and Di shall apply immediately after successful completion of the answer to reset;
- if b5=1 in TA(2), implicit values shall be used.

6.5.3 Extra guardtime N

Parameter N is the extra guardtime used to send characters from the interface device to the card. No extra guardtime is used to send characters from the card to the interface device. The default value is N = 0.

In the range 0 to 254, N indicates that, before being ready to receive the next character, the card requires the following delay from the leading edge of the previous character (sent either by the card or by the interface device).

$$12 \text{ etu} + \left(Q \times \frac{N}{f}\right)$$

In the formula, Q shall take either one of the two values:

— F/D, i.e., the values used for computing the etu, if T=15 is absent in the Answer-to-Reset;

— Fi/Di if T=15 is present in the Answer-to-Reset.

N=255 indicates that, during the transmission protocol, the minimum delay between the leading edges of two consecutive characters is the same in both directions of transmission. The value of this minimum delay is

— 12 etu for T=0,

— 11 etu for T=1.

Table 7 — Fi, indicated values of the clock rate conversion factor

FI	0000	0001	0010	0011	0100	0101	0110	0111
Fi	372	372	558	744	1116	1488	1860	RFU
f (max.) MHz	4	5	6	8	12	16	20	—

RFU = Reserved for Future Use

FI	1000	1001	1010	1011	1100	1101	1110	1111
Fi	RFU	512	768	1024	1536	2048	RFU	RFU
f (max.) MHz	—	5	7,5	10	15	20	—	—

Table 8 — Di, indicated values of the baud rate adjustment factor

DI	0000	0001	0010	0011	0100	0101	0110	0111
Di	RFU	1	2	4	8	16	32	RFU

DI	1000	1001	1010	1011	1100	1101	1110	1111
Di	12	20	RFU	RFU	RFU	RFU	RFU	RFU

6.5.4 Programming parameters P and I

Parameters P and I are respectively the programming voltage and the maximum programming current; they define the programming state on contact VPP.

— Programming voltage: V_{PP} = P V.

— Maximum programming current: I_{PP} = I mA.

In the range 5 to 25, PI1 gives the value P in volts. PI1=0 indicates that VPP is not electrically connected in the card which internally generates the programming power from the power supplied on contact VCC. Any other value of PI1 is reserved for future use.

In the range 50 to 250, PI2 gives the value P in decivolts. Any other value of PI2 is reserved for future use. If PI2 is present, the value of PI1 should be ignored.

If T=15 is absent in the Answer-to-Reset, the default values are P = 5 and I = 50. If T=15 is present, VPP is not connected in the card unless TB(1) and/or TB(2) is present.

Table 9 — Maximum programming current I

II	00	01	10	11
I	25	50	RFU	RFU

6.5.5 Clock stop indicator X

Parameter X indicates according to table 10 whether the card supports clock stop (XI≠00) or not (XI=00) and, when supported, which electrical state is preferred on CLK when the clock is stopped. The default value is X = "clock stop not supported".

Table 10 — Clock stop indicator X

XI	00	01	10	11
X	Not supported	State L	State H	No preference

6.5.6 Class indicator U

Parameter U indicates the class(es) of operating conditions accepted by the card. According to table 11, each bit of UI represents a class of operating conditions defined in 4.2.1: b1 for class A, b2 for class B. The default value is U = "only class A supported".

Table 11 — Class indicator U

UI	00 0001	00 0010	00 0011	Any other value
U	A only	B only	A and B	RFU

6.5.7 Specific mode byte TA(2)

TA(2) is the specific mode byte. According to figure 13, it describes the relevant features of the specific mode of operation of the card (see 6.6.2).

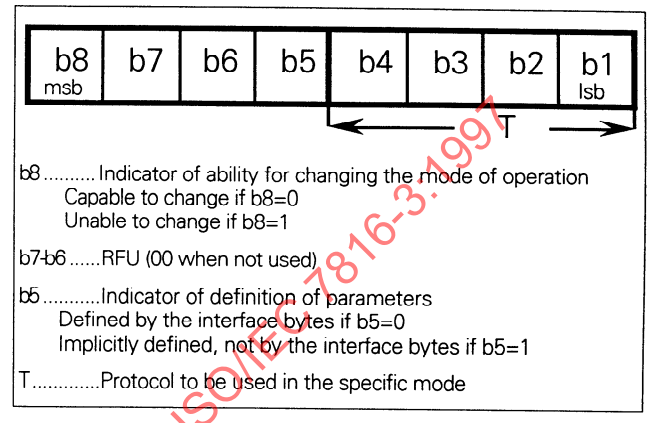

Figure 13 — Coding of TA(2)

6.6 Modes of operation

6.6.1 General overview

After the answer to reset, the card is in one of the following two modes of operation:

— either the specific mode if TA(2) is present,

— or the negotiable mode if TA(2) is absent.

Figure 14 shows selection and switching of modes of operation of the card.

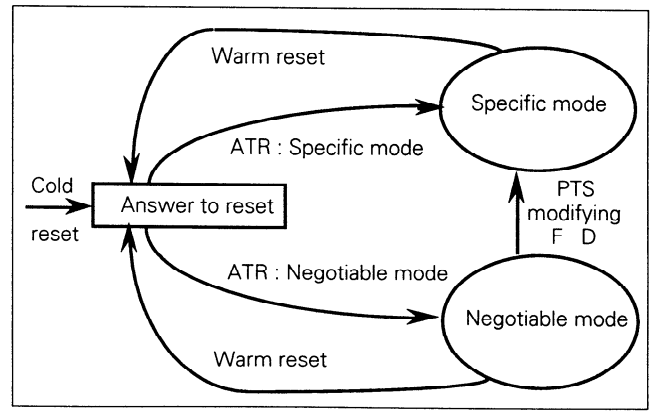

Figure 14 — Mode selection and switching

6.6.2 Specific mode

In the specific mode, directly after the answer to reset, the protocol indicated by TA(2) shall apply using for F and D (see 6.5.7):

— either the values Fi and Di if b5=0 in TA(2),

— or implicit values if b5=1 in TA(2).

However, the interface device may initiate a warm reset to invoke the negotiable mode in the card.

NOTES

1 If a card sends TA(2) to an interface device not aware of the existence of the specific mode, then the card cannot rely on an additional reset to switch to the negotiable mode.

2 If an interface device has detected a TA(2) byte, then the interface device should not issue a second reset before the answer to reset is completely received or the card has timed out.

6.6.3 Negotiable mode

In the negotiable mode, an "implicit selection" is possible as long as the first byte sent by the interface device to the card allows an unambiguous distinction between a PPS request and a command of the protocol.

— If no PPS request is sent directly after the answer to reset, then the "first offered protocol" (see 6.4.3.1) shall apply using Fd and Dd (see 6.5.2).

— For another protocol offered by the card and/or other values of parameters F and D in the ranges Fd to Fi and Dd to Di, the interface device shall send a PPS request using Fd and Dd to switch from the negotiable mode to the specific mode. Directly after a successful PPS exchange (see 7.4), the negotiated protocol shall apply using Fn and Dn.

If the Answer-to-Reset offers only one protocol (T=0 to 14) and only Fd and Dd, this protocol shall start using Fd and Dd immediately after the answer to reset. Consequently, such a card need not support PPS.

An interface device which supports neither PPS nor the "first offered protocol" may either reset the card to try to switch from the negotiable mode into a specific mode supported by the interface device or reject the card.

NOTES

1 A warm reset issued in the negotiable mode may switch the card into the specific mode.

2 If T=0 is present in a multi-protocol card, then T=0 is in the first position in the Answer-to-Reset. Therefore, in negotiable mode, only T=0 can be implicitly selected in such a card.

3 If either T=0 or T=1 is offered with values Fi and Di different from Fd and/or Dd, then the interface device may

- either select implicitly the protocol using Fd and Dd,
- or transmit a PPS request using Fd and Dd to negotiate other values Fn et Dn.

7 Protocol and parameters selection

7.1 General

This clause specifies an explicit protocol and parameters selection. This clause applies immediately after any answer to reset indicating the negotiable mode.

The PPS requests and responses shall be transmitted in the same way as the Answer-to-Reset, i.e., at the same baud rate (therefore using Fd and Dd), according to the convention set up by TS (see 6.4.1) and with the minimal delay of 12 etu between the leading edges of two consecutive characters. However if the interface byte TC(1) is present in the Answer-to-Reset with a value different from 'FF', the additional guardtime (see 6.5.3) shall be ensured. The delay between the leading edges of two consecutive characters of the PPS response shall not exceed the "initial waiting time" (see 6.3.2).

7.2 PPS protocol

Only the interface devices are permitted to start the PPS exchanges.

— The interface device shall send a PPS request to the card.

— If the card receives an erroneous PPS request, it shall not send any response.

— If the card receives a correct PPS request, it shall send a PPS response, if implemented, or the initial waiting time will be exceeded.

— If the initial waiting time is exceeded, the interface device shall either reset or reject the card.

— If the interface device receives an erroneous PPS response, it shall either reset or reject the card.

— If the PPS exchange is unsuccessful, then the interface device shall either reset or reject the card.

7.3 Structure and content of PPS request and response

The PPS request and PPS response each consist of one initial byte PPSS, followed by a format byte PPS0, three optional parameter bytes PPS1, PPS2, PPS3 and a check byte PCK as the last byte (see figure 15).

PPSS identifies the PPS request or response and is equal to 'FF'.

PPS0 indicates by the bits b5, b6, b7 equal to 1 the presence of the optional bytes PPS1, PPS2, PPS3, respectively. The bits b4 to b1 convey a value of parameter T to propose a protocol. The bit b8 is reserved for future use and shall be set to 0.

PPS1 allows the interface device to propose values of F and D to the card. Coded in the same way as in TA(1),

these values shall lie in the ranges Fd to Fi and Dd to Di respectively. If an interface device does not send PPS1, it proposes to continue with Fd and Dd. The card either acknowledges both values by echoing PPS1 (then these values become Fn and Dn) or does not send PPS1 to continue with Fd and Dd (then Fn is set to 372 and Dn to 1).

PPS2 and PPS3 are reserved for future use.

The value of PCK shall be such that the exclusive-oring of all the bytes PPSS to PCK inclusive is null.

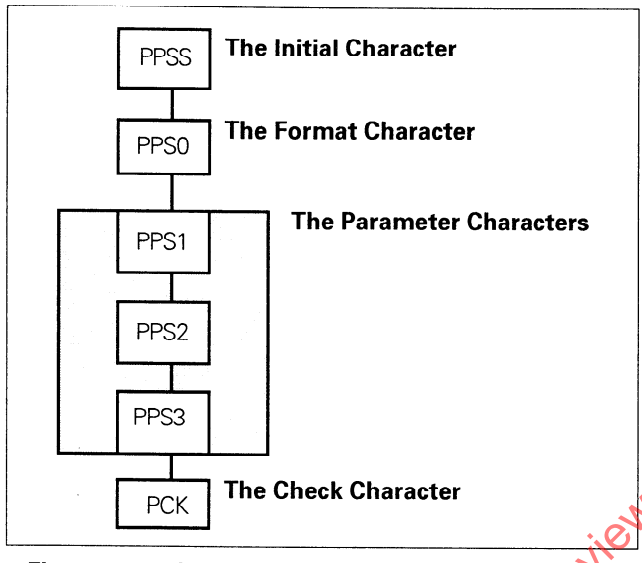

Figure 15 — Structure of PPS request and response

7.4 Successful PPS exchange

If the PPS response echoes exactly the PPS request, then the PPS exchange is successful. This is the most common case. However other cases may occur.

A PPS exchange is also successful when the PPS response is in the following conditions.

— PPSS_Response = PPSS_Request.

— PPS0_Response:

- The bits b1 to b4 shall be echoed.
- The bit b5 shall be either echoed or set to 0.
  If b5=1, PPS1_Response = PPS1_Request.
  If b5=0, PPS1_Response is not present, meaning that Fd and Dd shall be used.
- The bit b6 shall be either echoed or set to 0.
  If b6=1, PPS2_Response = PPS2_Request.
  If b6=0, PPS2_Response and PPS2_Request are both absent.
- The bit b7 shall be either echoed or set to 0.
  If b7=1, PPS3_Response = PPS3_Request.
  If b7=0, PPS3_Response and PPS3_Request are both absent.

Any other case of PPS exchange shall be interpreted as unsuccessful.

8 Protocol T=0, half-duplex transmission of asynchronous characters

8.1 Scope

This clause defines the structure and processing of commands in a half-duplex transmission of asynchronous characters. These commands are initiated by the interface device. This clause covers transmission control and card specific control.

The protocol starts after either the answer to reset (see 6) or a successful PPS exchange (see 7).

8.2 Character level

The character frame is as defined for the answer to reset in 6.3, using the convention set up by TS in 6.4.1, taking into account 6.5.2 and 6.5.3 according to the mode of operation in 6.6. The card and the interface device shall use the error signal and character repetition according to 6.3.3.

Any transition on VPP triggered by a procedure byte shall occur within 12 etu from the character leading edge.

The specific interface byte TC(2) codes the integer value WI over the eight bits; the null value is reserved for future use. If no TC(2) appears in the Answer-to-Reset, then the default value is WI = 10. The interval between the leading edge of any character sent by the card and the leading edge of the previous character (sent either by the card or by the interface device) shall not exceed 960 x WI x (Fi / *f*). This maximum delay is named the "work waiting time".

On the work waiting time overflow, VPP shall be set to or maintained at pause state.

8.3 Structure and processing of commands

8.3.1 General overview

The interface device initiates every command by sending a five-byte header which tells the card what to do. The command processing continues with the transfer of a variable number of data bytes in one direction under the control of procedure bytes sent by the card.

It is assumed that the card and the interface device know a priori the direction of transfer, in order to distinguish

— commands for incoming data transfers where the data bytes enter the card while processing and

— commands for outgoing data transfers where the data bytes leave the card while processing.

8.3.2 Command header

The header is a sequence of five bytes designated CLA, INS, P1, P2, P3.

— CLA is an instruction class. The value 'FF' is reserved for PPS (see 6.6.3).

— INS is an instruction code in the instruction class. The instruction code is valid only if the bits b8 to b5 are not equal to either '6' or '9'.

— P1 P2 are a reference (e.g., an address) completing the instruction code.

— P3≠0 codes the number n of data bytes denoted as D(1) to D(n) to be transferred during the command.
- In an outgoing data transfer command, P3=0 introduces a 256-byte data transfer from the card.
- In an incoming data transfer command, P3=0 introduces no data transfer.

All remaining encoding possibilities for the header are reserved for other parts of ISO/IEC 7816. After transmitting the header, the interface device shall wait for a character conveying a procedure byte.

8.3.3 Procedure bytes

8.3.3.1 General

There are three types of procedure bytes (see table 12).

— NULL is equal to '60'.

— In ACK, the bits b8 to b2 are all equal or all complementary to those of INS, apart from the values '6X' and '9X'.

— SW1 is equal to '6X' or '9X', except for '60'.

At each procedure byte, the card can proceed with the command by NULL or ACK, or conclude by an end sequence SW1 SW2, or show its disapproval by becoming unresponsive.

8.3.3.2 Null byte

NULL requests no further action neither on VPP state nor on data transfer. The interface device shall only wait for a character conveying a procedure byte.

8.3.3.3 Acknowledge bytes

ACK is used to control data transfer and VPP state (see 4.3.6, table 6 and 6.5.4).

— If exclusive-oring ACK and INS gives '00' or 'FF', then VPP shall be set to or maintained at pause state.

— If exclusive-oring ACK and INS gives '01' or 'FE', then VPP shall be set to or maintained at programming state.

— If the bits b8 to b2 in ACK have the same value as those in INS, then all remaining data bytes, D(i) to D(n), if any remain, shall be transferred subsequently.

— If the bits b8 to b2 in ACK are complementary to those in INS, then only the next data byte, D(i), if one remains, shall be transferred.

After these actions, the interface device shall wait for a character conveying a procedure byte.

8.3.3.4 Status bytes

SW1 requests VPP to be set to or maintained at pause state. The interface device shall wait for a character conveying a SW2 byte. There is no restriction on SW2 value.

SW1 SW2 form the end sequence indicating the card status at the end of the command. The normal ending is indicated by SW1 SW2 = '9000'.

This part of ISO/IEC 7816 does not interpret the other end sequences where the bits b8 to b5 of SW1 are equal to '9'; their meaning relates to the application itself.

If the bits b8 to b5 are equal to '6', then the meaning of SW1 is independent of the application. ISO/IEC JTC 1 SC 17 reserves for future use those values, apart from the following five values.

'6E' The card does not support the instruction class.

'6D' The instruction code is not programmed or is invalid.

'6B' The reference is incorrect.

'67' The length is incorrect.

'6F' No precise diagnosis is given.

If SW1 is neither '6E' nor '6D', then the card supports the instruction.

Table 12 — Procedure bytes

Byte	Value	Result on VPP	Result on data transfer	Then reception of
NULL	'60'	No action	No action	A procedure byte
ACK	INS	Pause state	All remaining data bytes	A procedure byte
	INS ⊕ '01'	Programming state	All remaining data bytes	A procedure byte
	INS ⊕ 'FF'	Pause state	The next data byte	A procedure byte
	INS ⊕ 'FE'	Programming state	The next data byte	A procedure byte
SW1	'6X' (≠'60'), '9X'	Pause state	No action	A SW2 byte

9 Protocol T=1, half-duplex asynchronous transmission of blocks

9.1 Scope and principles

This clause defines the structure and processing of commands in an half-duplex asynchronous transmission of blocks. The interface device and the card may initiate these commands. This clause covers card specific control and data transmission control such as flow control, block chaining and error correction.

The protocol starts after either the answer to reset (see 6) or a successful PPS exchange (see 7). The main characteristics of the protocol are the following.

— The protocol starts with a first block sent by the interface device; the protocol continues with alternating the right to send a block.

— A block is the smallest data unit which can be exchanged. A block may be used to convey

- application data transparent to the protocol,
- transmission control data including transmission error handling.

— The block structure allows to check the received block before processing the conveyed data.

The protocol applies the principle of layering of the OSI reference model. A particular attention has minimized interactions across boundaries. Three layers are defined.

— The physical layer transmits moments organized in asynchronous characters according to 9.3.

— The data link layer includes a character component and a block component.

- The character component handles the block identification (recognizing the start and the end of a block) and ensures controls according to 9.6.
- The block component exchanges blocks according to 9.7.

— The application layer processes commands, which involves the exchange of at least one block or chain of blocks in each direction.

9.2 Terms and definitions

For the purposes of this clause, the following definitions apply.

9.2.1
block
sequence of bytes comprising two or three fields defined as prologue field, information field and epilogue field

9.2.1.1
information block
block whose primary purpose is to convey application layer information

9.2.1.2
receive ready block
block conveying the number of the expected I-block, used as a positive or negative acknowledgment

9.2.1.3
supervisory block
block conveying transmission control information

9.2.2
error detection code
content of the epilogue field, resulting from an error checking method applied to all bytes in the prologue field and in the information field

9.2.3
field
one of the three components of the block, defined as prologue field, information field and epilogue field

9.2.3.1
prologue field
first field of a block, conveying the subfields: node address byte, protocol control byte and length byte

9.2.3.2
information field
field of a block, conveying data, generally application data

9.2.3.3
epilogue field
final field of a block, conveying the error detection code

9.2.4
subfield
functional component of a field

9.2.4.1
node address byte
subfield of the prologue field, indicating both destination and source addresses of the block and controlling VPP state

9.2.4.1.1
destination node address
portion of the subfield node address, identifying the intended receiver of the block

9.2.4.1.2
source node address
portion of the subfield node address, identifying the sender of the block

9.2.4.2
protocol control byte
subfield of the prologue field, containing transmission control information

9.2.4.3
length byte
subfield of the prologue field, containing the number of bytes transmitted in the information field of the block

9.2.5
transmission control
function used to control the data transmission between the interface device and the card, including VPP state control, block transmission with sequence control, synchronization and recovery of transmission errors

For the purposes of this clause, the following abbreviations apply.

BGT	block guardtime
BWI	block waiting time integer
BWT	block waiting time
CRC	cyclic redundancy check
CWI	character waiting time integer
CWT	character waiting time
DAD	destination node address
EDC	error detection code
I-block	information block
IFS	maximum information field size
IFSC	IFS for the card
IFSD	IFS for the interface device
INF	information field
LEN	length byte
LRC	longitudinal redundancy check
NAD	node address byte
OSI	open systems interconnection
PCB	protocol control byte
R-block	receive ready block
R	receive ready
SAD	source node address
S-block	supervisory block
WTX	waiting time extension

9.3 Character frame

The character frame is as defined for the answer to reset in 6.3 (except for 6.3.3), using the convention set up by TS in 6.4.1, taking into account 6.5.2 and 6.5.3 according to the mode of operation in 6.6.

The error signal and character repetition according to 6.3.3 shall not be used, so that the minimum delay between the leading edges of two consecutive characters of a block may be reduced to 11 etu, according to the interface byte TC(1) specified in 6.5.3.

Character parity allows to check a block in addition to the error detection code (see 9.4.4 and 9.5.4).

9.4 Block frame

9.4.1 General

A block is a sequence of bytes: each byte is conveyed in an asynchronous character. As shown in figure 16, a block consists of the following fields.

— The prologue field is mandatory; it consists of a node address byte, a protocol control byte and a length byte.

— The information field is optional; it consists of zero to 254 bytes.

— The epilogue field is mandatory; it consists of one or two bytes.

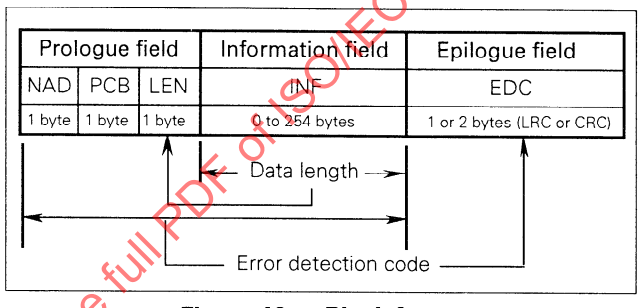

Figure 16 — Block frame

The protocol defines three types of blocks.

— An information block (I-block) is used to convey information for use by the application layer. In addition, it conveys a positive or negative acknowledgment.

— A receive ready block (R-block) is used to convey a positive or negative acknowledgment. Its information field shall be absent.

— A supervisory block (S-block) is used to exchange control information between the interface device and the card. Its information field may be present depending on its controlling function.

NOTE — This separation allows the design of the protocol control and the application portions of the device microcode to be relatively independent of one another.

9.4.2 Prologue field

9.4.2.1 Node address byte

NAD allows to identify the source and the intended destination of the block; it may be used to distinguish between multiple logical connections when they coexist.

The bits b1 to b3 are the source node address SAD and the bits b5 to b7 the destination node address DAD. The bits b4 and b8 are used for VPP state control (see 9.6.1).

When the addressing is not used, the values of SAD and DAD shall be set to 0. Any other value of NAD where SAD and DAD are identical is reserved for future use.

In the first block sent by the interface device, NAD shall set up a logical connection by associating the addresses SAD and DAD. Subsequent blocks in which NAD contains the same pair of addresses SAD and DAD are associated with the same logical connection. During information exchange, other logical connections may be set up by other pairs of addresses SAD and DAD.

NOTE — For example, blocks sent by the interface device with the values x for SAD and y for DAD and blocks sent by the card with the values y for SAD and x for DAD belong to a logical connection denoted by (x, y), whereas blocks sent by the interface device with the values v for SAD and w for DAD and blocks sent by the card with the values w for SAD and v for DAD belong to another logical connection (v, w).

9.4.2.2 Protocol control byte

PCB conveys information required to control transmission. PCB defines whether a block is an I-block, an R-block or an S-block.

— In the PCB of every I-block, the bit b8 is set to 0. The bits b7 b6 are used as shown in figure 17. The bits b5 to b1 are reserved for future use and shall be set to 0.

— In the PCB of every R-block, the bits b8 b7 are set to 10. The bits b6 to b1 are used as shown in figure 18.

— In the PCB of every S-block, the bits b8 b7 are set to 11. The bits b6 to b1 are used as shown in figure 19.

9.4.2.3 Length byte

LEN indicates the number of bytes present in the information field of the block (see also 9.5.2).

The coding for LEN shall be the following.

— The value '00' indicates that the information field is absent.

— Any value from '01' to 'FE' is the number of bytes present in the information field, from 1 to 254.

— The value 'FF' is reserved for future use.

9.4.3 Information field

The use of INF depends upon the block type.

— When present in an I-block, INF conveys application information.

— INF shall be absent in an R-block.

— When present in an S-block, INF conveys non application information.

- INF shall be present with a single byte in an S-block adjusting IFS and WTX.
- INF shall be absent in an S-block signalling an error on VPP state or managing chain abortion or resynchronization.

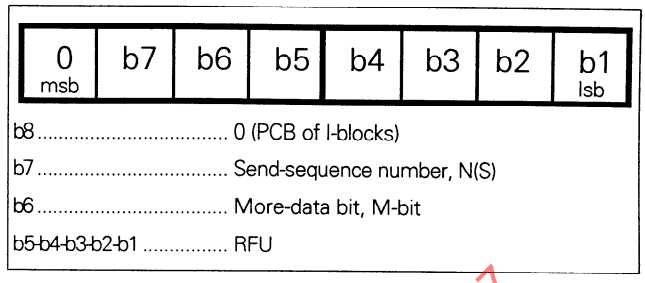

Figure 17 — Coding of I-block PCB

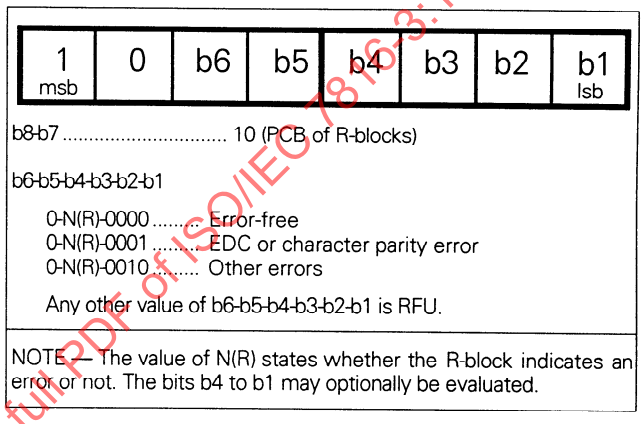

Figure 18 — Coding of R-block PCB

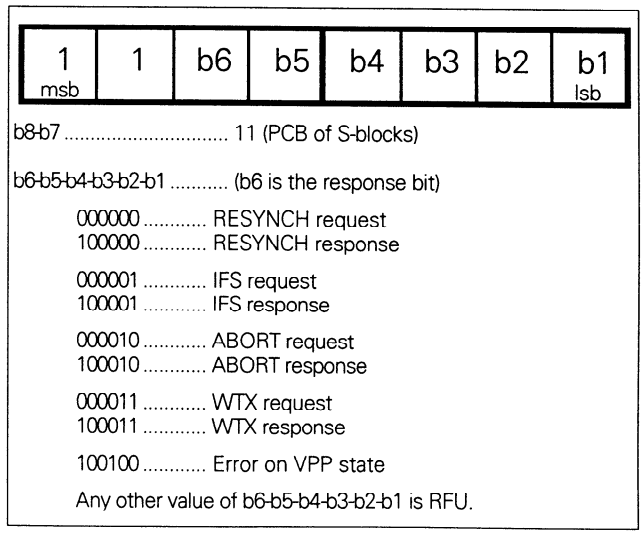

Figure 19 — Coding of S-block PCB

9.4.4 Epilogue field

EDC conveys the error detection code of the block. The protocol uses either a LRC or a CRC.

— The longitudinal redundancy check (LRC) consists of one byte. Its value shall be such that the exclusive-oring of all the bytes of the block is null.

— The cyclic redundancy check (CRC) consists of two bytes. For its value, see ISO/IEC 3309.

9.5 Protocol parameters

9.5.1 Specific interface bytes for T=1

If present in the Answer-to-Reset after the first occurrence of T=1 in TD(i–1) for i > 2, the specific interface bytes TA(i) TB(i) TC(i) are used to set up the protocol parameters at non-default values.

For notation simplicity, these three bytes are hereafter named the first TA(i), the first TB(i) and the first TC(i).

9.5.2 Information field sizes

9.5.2.1 IFS for the card

IFSC is the maximum length of information field of blocks which can be received by the card. The initial value of IFSC is set up by the first TA(i) with 32 as default value.

9.5.2.2 IFS for the interface device

IFSD is the maximum length of information field of blocks which can be received by the interface device. The initial value of IFSD is 32.

9.5.2.3 Coding for IFSC and IFSD

At the start of the protocol, IFSC and IFSD are initialized. During the protocol, IFSC and IFSD may be adjusted by S(IFS request) and S(IFS response) where INF consists of one byte named IFS. In any case, the first TA(i) and the bytes IFS shall be coded as follows.

— The values '00' and 'FF' are reserved for future use.

— The values '01' to 'FE' are the numbers 1 to 254.

NOTE — The block size is the total number of bytes present in the prologue, information and epilogue fields. The maximum block size is equal to IFS plus four or five, depending upon the length of the epilogue.

9.5.3 Waiting times

9.5.3.1 Character waiting time

CWT is defined as the maximum delay between the leading edges of two consecutive characters in the block (see figure 20).

NOTE — When there is a potential error in the length, CWT may be used to detect the end of a block.

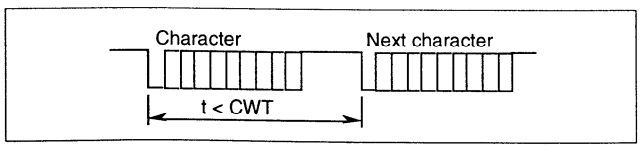

Figure 20 — Character waiting time

The bits b4 to b1 of the first TB(i) give CWI from 0 to 15. The default value of CWI is 13. CWT is calculated from CWI by the following formula.

$$CWT = (11 + 2^{CWI}) \text{ etu}$$

Therefore the minimum value of CWT is 12 etu.

9.5.3.2 Block waiting time

BWT is defined as the maximum delay between the leading edge of the last character of the block received by the card and the leading edge of the first character of the next block sent by the card (see figure 21). BWT is used to detect an unresponsive card.

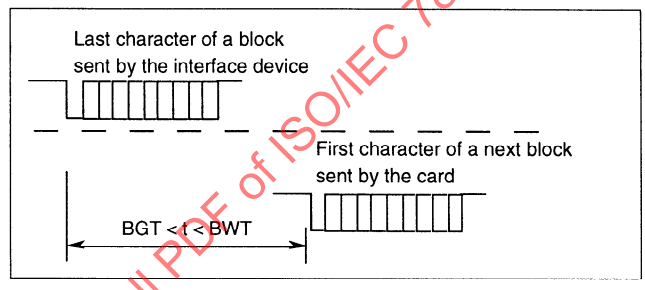

Figure 21 — Block waiting time and block guardtime

The bits b8 to b5 of the first TB(i) give BWI from 0 to 9. The values 10 to 15 are reserved for future use. The default value of BWI is 4. BWT is calculated from BWI by the following formula.

$$BWT = 11 \text{ etu} + 2^{BWI} \times 960 \times \frac{372}{f} \text{ s}$$

9.5.3.3 Block guardtime

BGT is defined as the minimum delay between the leading edges of two consecutive characters sent in opposite directions. The value of BGT shall be 22 etu.

Consequently, the delay between the last character of a block received by the card and the first character of the next block sent by the card shall be at least BGT but at most BWT (see figure 21).

9.5.4 Error detection code

The bit b1 of the first TC(i) indicates the error detection code to be used:

— CRC if b1=1;

— LRC (default value) if b1=0.

The bits b8 to b2 are reserved for future use and shall be set to 0.

9.6 Character component operation at data link layer

9.6.1 VPP state control

VPP state (see 4.3.6, table 6 and 6.5.4) is managed by the interface device under the control of NAD and PCB characters sent by the card. Bits b8 and b4 of the NAD byte shall be used as follows.

b8=0, b4=0
VPP shall be set to or maintained at pause state.

b8=1, b4=0
VPP shall be set to programming state until reception of the PCB character.

b8=0, b4=1
VPP shall be set to programming state until reception of another NAD character.

b8=1, b4=1
This coding is forbidden.

If a parity error occurs on the NAD character, VPP shall be set to or maintained at pause state.

If a time-out occurs, i.e., if the card fails to send an expected character within CWT or BWT, VPP shall be set to or maintained at pause state.

Any transition on VPP triggered by a character shall occur within 12 etu from the character leading edge.

9.6.2 Error-free operation

At the beginning of the protocol, the interface device has the right to send. When T=1 has been selected, the interface device sends only blocks.

When either the card or the interface device has sent a block, it switches to reception mode. When either the card or the interface device has received the number of bytes according to the length subfield, it assumes that it has the right to send.

9.7 Block component operation at data link layer

9.7.1 Notations

The following notations are used in the descriptions of the protocol.

I-blocks are denoted as follows.

I(N(S), M)
I-block where N(S) is the send-sequence number of the block and where M is the more-data bit (see 9.7.2.2)

$N_a(S)$, $N_b(S)$
send-sequence numbers of I-blocks where indices a and b distinguish sources A and B

R-blocks are denoted as follows.

R(N(R))
R-block where N(R) is the number of the expected I-block

S-blocks are denoted as follows.

S(RESYNCH request)
S-block requesting a resynchronization

S(RESYNCH response)
S-block acknowledging the resynchronization

S(IFS request)
S-block offering a maximum size of the information field

S(IFS response)
S-block acknowledging IFS

S(ABORT request)
S-block requesting a chain abortion

S(ABORT response)
S-block acknowledging the chain abortion

S(WTX request)
S-block requesting a waiting time extension

S(WTX response)
S-block acknowledging the waiting time extension

S(Error on VPP state)
S-block informing the card of a VPP state error

S(IFS...) and S(WTX...) contain INF, whose coding is defined by rules 3 and 4 in 9.7.2.3.