

PUBLICLY
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SPECIFICATION

IEC
PAS 62326-7-1

First edition
2007-04

**Performance guide for single-
and double-sided flexible
printed wiring boards**



JPCA

Reference number
IEC/PAS 62326-7-1:2007(E)



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Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE

X

For price, see current catalogue

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PERFORMANCE GUIDE FOR SINGLE- AND DOUBLE-SIDED FLEXIBLE PRINTED WIRING BOARDS

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The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Draft PAS	Report on voting
91/615A/NP	91/643/RVN

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard

This PAS shall remain valid for an initial maximum period of three years starting from 2007-04. The validity may be extended for a single three-year period, following which it shall be revised to become another type of normative document or shall be withdrawn.

PERFORMANCE GUIDE FOR SINGLE- AND DOUBLE-SIDED FLEXIBLE PRINTED WIRING BOARDS

1 Scope

This PAS provides the requirements for the single- and double-sided flexible printed wiring boards (hereinafter designated as "flexible printed board" or FPC).

In this document, an FPC means a single- or double-sided FPC prepared by lamination of a film of polyester or polyimide with copper foil(s) on one or both sides of a board including the type with no adhesive layer, and with conductor pattern formed by the subtractive method (etching of the copper foil), or possibly by the build-up method.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60326-7:1981, *Printed boards – Part 7: Specification for single- and double-sided flexible printed boards without through connections*

IEC 60326-8:1981, *Printed boards – Part 8: Specification for single- and double-sided flexible printed boards with through connections*

JPCA-TD01:2000, *Terms and definitions for printed circuits*

JPCA-BM03:2003, *Flexible printed wiring boards (adhesive and adhesiveless types)*

JIS C 5016:1994, *Test methods for flexible printed wiring boards*

JIS C 5017:1994, *Single- and double-sided flexible printed wiring boards*

JIS C 5603:1993, *Terms and definitions for printed circuits*

JIS C 6471:1995, *Test methods of copper-clad laminates for flexible printed wiring boards*

JIS C 6472:1995, *Copper-clad laminates for flexible printed wiring boards (polyester film, polyimide film)*

JIS C 6515:1998, *Copper foil for printed wiring boards*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in JIS C 5603, JIS C 5017, JIS C 5016, and JPCA-FC03 apply.

4 Test methods

The test methods used in this document as specified below shall be in conformance with JIS C 5016.

- a) Test methods requiring complicated referencing procedures are reproduced in this document.
- b) Tests on through connection apply only to double-sided FPCs.

- c) External appearance is the only requirement specified in this document for stiffeners affixed to FPCs.

5 Performance levels

The FPCs are classified into three levels, Levels 1, 2, and 3, and an additional special level, Level X, for applications requiring special attention. They are defined as:

Level 1 – FPCs requiring "ordinary" performance;

Level 2 – FPCs requiring "high" performance;

Level 3 – FPCs requiring "extra-high" performance;

Level X – FPCs requiring special performances which do not belong to the above-mentioned three levels, and the specifications requiring an agreement between user and supplier.

A relevant level of the board is chosen for a specific application of the board. A different level can be selected for a specific section of the board when the required specification of the section is different from that of another part of the board.

6 Base materials

The base materials used in FPCs shall satisfy the requirements specified in JPCA-BM03.

7 Visual inspection

7.1 Test environment

The test environment shall meet the requirements of JIS C 5016, Clause 3.

7.2 Test specimens

The test specimens shall meet the requirements of JIS C 5016, Clause 4.

7.3 Tools for testing

A magnifying glass having a magnification of 3× to 10× shall be used for examining the appearance and the surface finish conditions of the product. Dimensions shall be measured with a scaled magnifying glass or an instrument capable of two-dimensional coordinate measuring, if necessary. Thickness shall be measured with a micrometer having an accuracy of 1 μm or better.

7.4 Preparation of limit samples

Limit samples showing the required criteria to make technical judgments may be prepared under agreement between user and supplier for the application of this document.

7.5 Description of inspection

Requirements, procedures, and illustration for visual inspections are given in 7.5.1 through 7.5.6. Requirements that are not designated for a specific performance level shall apply to all the performance Levels 1, 2 and 3.

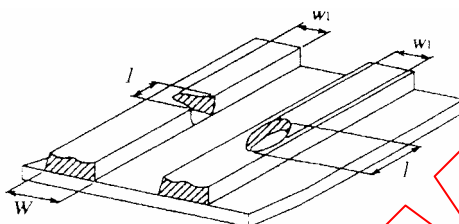
7.5.1 Visual inspection of conductor

7.5.1.1 Open and short circuit

There shall be no open and/or short circuit on FPCs.

7.5.1.2 Nicks and pinholes on conductor

- a) The allowable width (w_1) and length (l) of a nick and a pinhole of the conductor reducing conductor width, as shown in Figure 1, shall meet the requirement given in Table 1 for the finished conductor width (W) (see Note 1).



NOTE 1 The width of the finished conductors should be measured at the bottom of the conductor.

Figure 1 – Nicks and pinholes in conductor

Table 1 – Allowable nicks and pinholes

Level	Nicks and pinholes
1 and 2	$w_1 \leq 1/2 W$ $l \leq 2 W$
3	$w_1 \leq 1/3 W$ $l \leq W$

- b) The void area on a land, as illustrated in Figure 2, shall not exceed 10 % of the effective exposed land area.

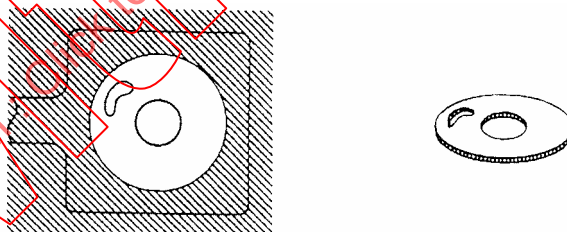


Figure 2 – Reduced area on land

- c) The circumferential void of a lead insertion hole, as illustrated in Figure 3, shall not exceed one-third of the total circumference.

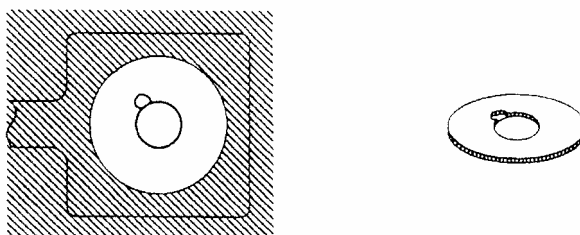


Figure 3 – Circumferential void at the component hole

7.5.1.3 Distance between conductor/spur and nodule of conductor

The distance (s_1) or ($s_2 + s_3$) in Figure 4 relative to the finished conductor spacing(s) shall meet the requirement given in Table 2.

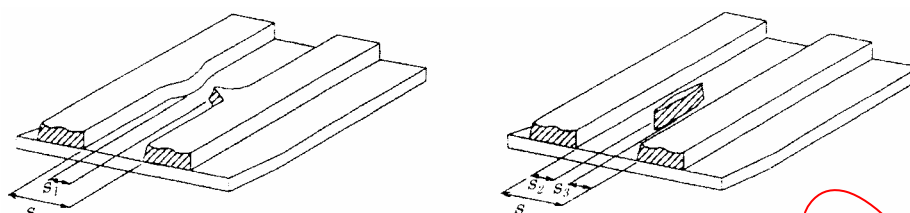


Figure 4 – Unnecessary copper between conductor/spur and nodule of conductor

Table 2 – Allowable unnecessary copper, spur and nodule between conductors

Level	Unnecessary copper, spurs and nodules, s_1 or ($s_2 + s_3$)
1 and 2	$1/2 s_1 \leq a$ or ($s_2 + s_3$)
3	$2/3 s_1 \leq a$ or ($s_2 + s_3$)

7.5.1.4 Unnecessary copper between conductor/spur and nodule of conductor in an open area

The spacing(s) between the board edges and the unnecessary copper or spur and nodule shall be larger than 0,125 mm in an open area where no conductor pattern is routed, as illustrated in Figure 5. The spacing(s) between the board edge and the unnecessary copper or spur and nodule shall be larger than 0,125 mm. The open area as stated in this clause shall have a width of no less than 0,375 mm.

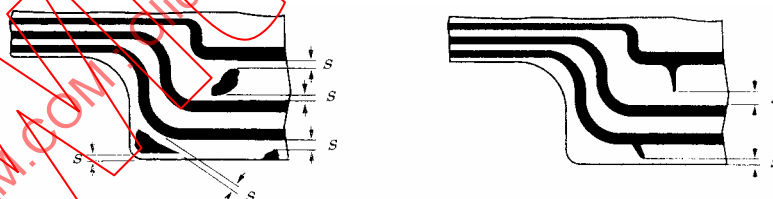


Figure 5 – Unnecessary copper, spurs and nodules in an open area and nodules of conductor corners

7.5.1.5 Etched concave surface of the conductor

Etched concave surface (d) of the conductor relative to the conductor thickness (t), as illustrated in Figure 6, shall meet the requirement given in Table 3. The concave surface shall not run across the entire width of a conductor.

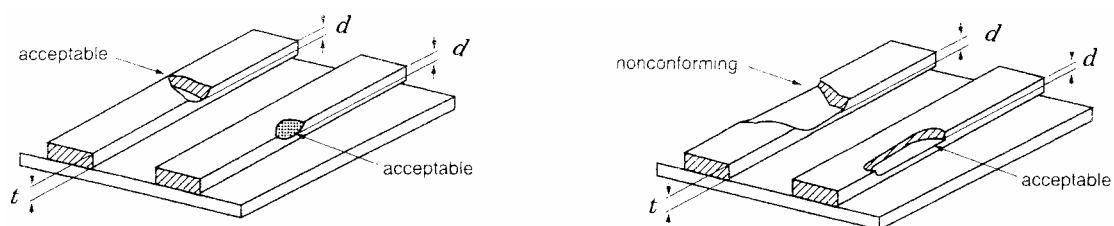


Figure 6 – Etched concave surface of the conductor and nodule at a conductor corner

Table 3 – Allowable etched concave of the surface conductor

Level	Etched concave surface of the conductor, d (t : conductor thickness)
1 and 2	$d \leq 1/3 t$
3	$d \leq 1/5 t$

7.5.1.6 Conductor delamination

The width (w_1) and length (l) of conductor delamination relative to the finished conductor width (W), as illustrated in Figure 7, shall meet the requirement given in Table 4.

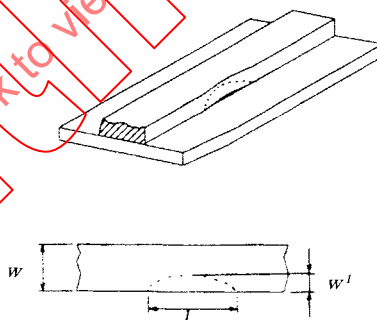


Figure 7 – Conductor delamination

Table 4 – Allowable conductor delamination

Level	Conductor delamination, length (l), width (w_1)
1	Coverlay laminated area $l \leq W$ and $w_1/W \leq 1/3$ for flexing area $l \leq W$ and $w_1/W \leq 1/2$ for other area
	No coverlay laminated area $l/W \leq 1/4$ and $w_1/W \leq 1/4$
2 and 3	There shall be no delamination in the conductor which can be observed by the naked eye

7.5.1.7 Conductor crack

There shall be no crack in the conductor.

7.5.1.8 Scratch on conductor

A scratch on a conductor surface, as illustrated in Figure 8, indicates the damage made by a sharp metal point and is harmful to the performance of the printed circuit. The depth (d) of a scratch shall meet the requirement given in Table 5 relative to the conductor thickness (t). The scratch shall not damage the bending property of the repeatedly flexing portion.

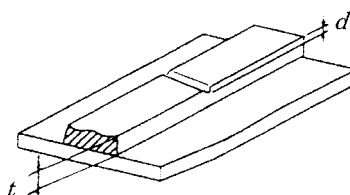


Figure 8 – Scratch on conductor

Table 5 – Allowable scratch on conductor

Level	Depth of scratch on conductor, d
1 and 2	$d \leq 1/3 t$
3	$d \leq 1/5 t$

7.5.1.9 Discoloration

Discoloration shall meet the requirement given in Table 6.

Table 6 – Allowable discoloration

Level	Discoloration
1 and 2	When discoloration is observed on a conductor laminated with coverlay, the discoloration shall be acceptable unless it is remarkably noticeable after conditioning at 40 °C with 90% RH for 96 h
3	The acceptable discoloration shall be agreed upon between user and supplier by means of a limit sample

7.5.2 Visual inspection of coverlay and covercoat

7.5.2.1 Void

Void, as illustrated in Figure 9, shall meet the requirement given in Table 7.

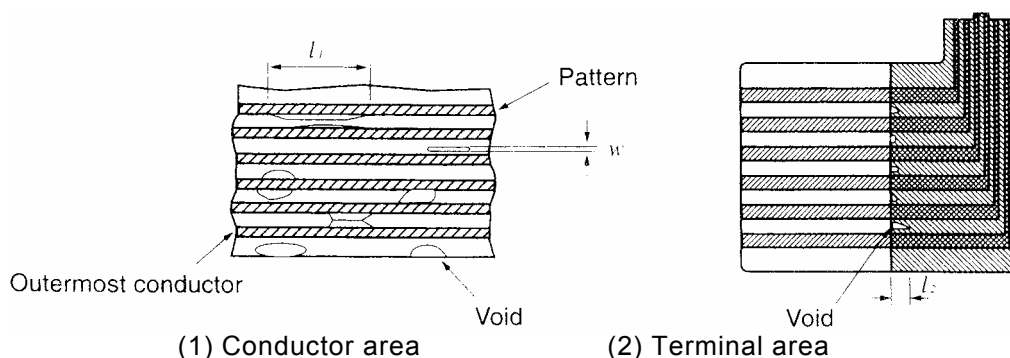


Figure 9 – Voids

Table 7 – Allowable void

Level	Voids
1	A void extending over two or more conductors shall not exist. A void both on the outline edge and to a conductor shall not exist. (A void at the terminal area, as illustrated in Figure 9 (2), shall be acceptable even if it extends to two conductors) The maximum length (l_2) of a void shall be 0,3 mm
2	The length of a void (l_1) shall be no longer than 10 mm. The width of a void (w) shall be no longer than one-third of the spacing between the conductors. There shall be no void in a contact extending to two neighbouring conductors. The maximum length (l_2) of a void shall be 0,3 mm. A void at the repeatedly bending area shall not damage the flexibility of the board
3	There shall be no void

7.5.2.2 Foreign substance

Foreign substance, as illustrated in Figure 10, shall meet the following requirements.

- Conductive foreign substance:** Requirements 7.5.1.3 and 7.5.1.4 of this specification shall apply to conductive foreign substances.
- Non-conductive foreign substance:** Non-conductive foreign substances shall meet the requirement given in Table 8.

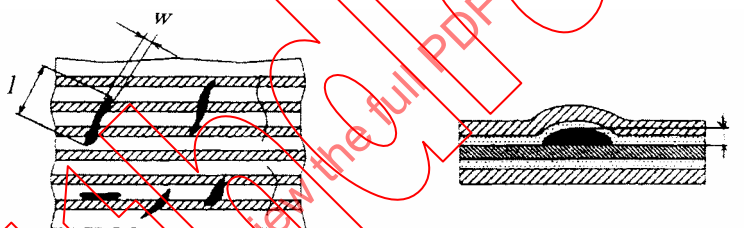


Figure 10 – Foreign substance

Table 8 – Allowable non-conductive foreign substance

Unit: mm			
Level	Thickness t	Width w	Length l
Level 1	$t \leq 0,1$	$w \leq 0,3$	$l \leq 3$
Level 2	$t \leq 0,05$	$w \leq 0,2$	$l \leq 2$
Level 3	$t \leq 0,05$	$w \leq 0,05$	$l \leq 1$
A foreign substance shall not extend to three or more conductors			

7.5.2.3 Blistering and delamination

There shall be no visible blistering and delamination of coverlay or covercoat along the edge of the FPC, as illustrated in Figure 11. The covercoat shall not be peeled off when using the test tape specified in JIS C 5016, 8.5.1.

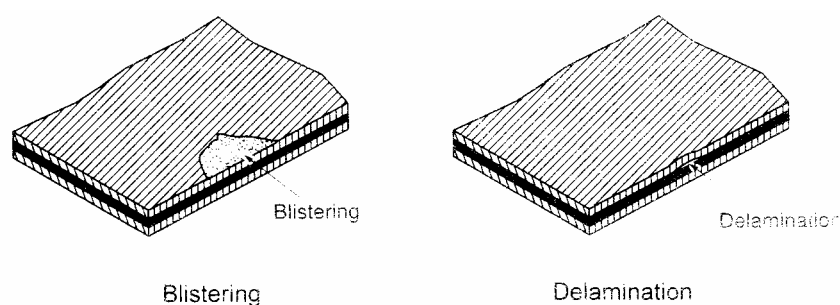


Figure 11 – Lifting and delamination of coverlay and covercoat

7.5.2.4 Squeeze-out of adhesive of coverlay, ooze-out of covercoat and photosensitive register strike

Squeeze-out of adhesive, ooze-out (l) of covercoat and photosensitive register strike, as illustrated in Figure 12, shall comply with the specification given in Table 9.

The squeeze-out and ooze-out at a land as illustrated in Figure 12-1 shall comply with the specification given in Table 10 for the effective land width (w), including possible printing and/or punching errors.

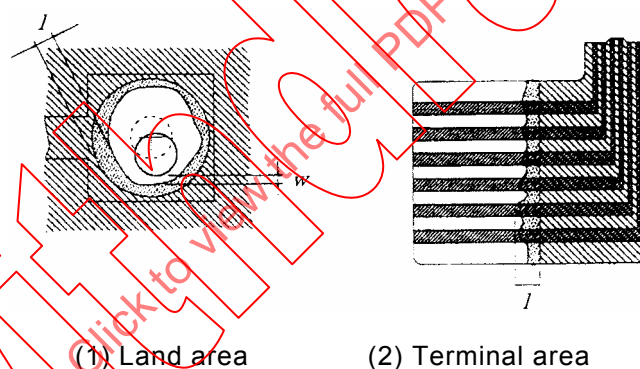


Figure 12 – Allowable squeeze-out of coverlay adhesive and ooze-out of covercoat and photosensitive resist

Table 9 – Allowable squeeze-out of coverlay adhesive, and ooze-out of covercoat and photosensitive register strike

Unit: mm

Level	Squeeze-out of coverlay adhesive and ooze-out of covercoat	Ooze-out of a photosensitive register strike
1 and 2	$l \leq 0,3$	—
3	$l \leq 0,2$	$l \leq 0,1$
3	$\leq 0,2$	$\leq 0,1$

Table 10 – Effective land width at a land

Level	Effective land width, w
1	Squeeze-out/ooze-out contacting the hole edge is acceptable up to one-third of the terminal hole circumference
2	0,05 mm min.
3	0,1 mm min.

7.5.2.5 Skipping of covercoat photosensitive register strike

When tested in accordance with JIS C 5016, 10.4, no solder shall stick onto the conductor of the covercoat and photoresist in the skipped area.

7.5.3 Visual inspection of plating

7.5.3.1 Plating defect

Plating defect shall meet the requirements given in 7.5.3.1.1 and 7.5.3.1.2.

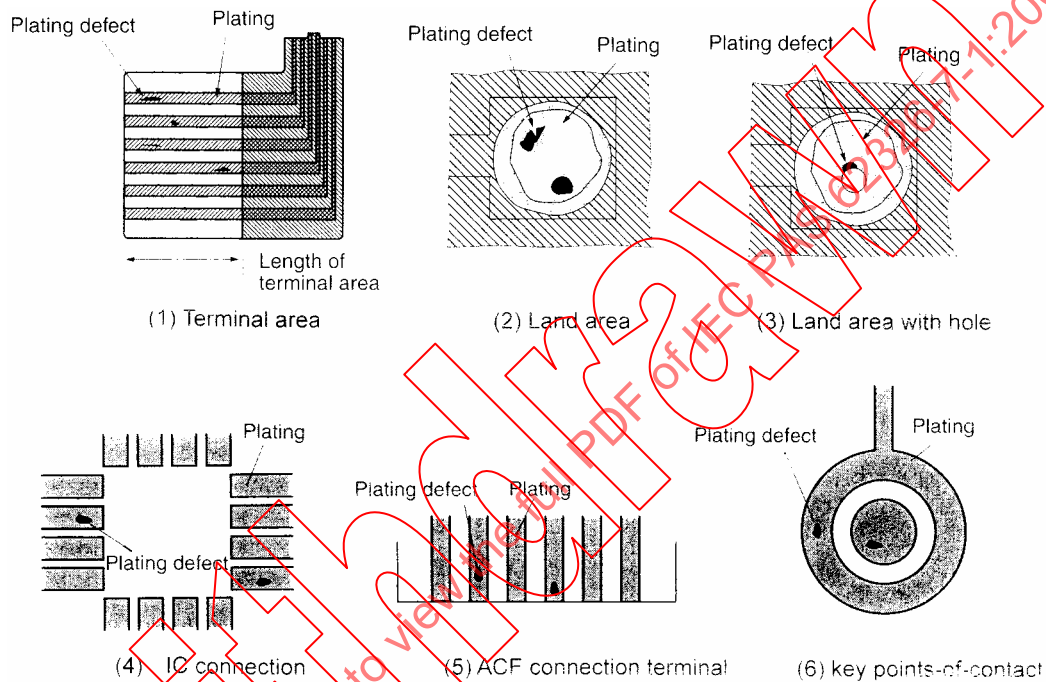
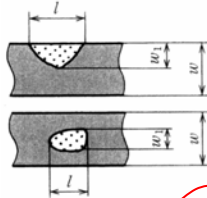


Figure 13 – Plating defects

7.5.3.1.1 Gold plating

Gold plating shall meet the requirement given in Table 11.

Table 11 – Gold plating

Level	Gold plating	Examples in Figure 13																	
1	Plating defects on the land area, as shown in Figure 13 (2) and (3) shall be no larger than 10 % of the total plated area (excluding the skipped plating area for a defect caused by adhesive squeeze-out)	(2), (3)																	
2	<p>The width (w_1) and length (l) of the plating defects in comparison to the finished line conductor width (w) are specified in the table below</p> <div></div> <p>Width and length of plating defects</p> <p>Unit: mm</p> <table><tr><th colspan="2" rowspan="2">Item</th><th colspan="3">Finished line width, w</th></tr><tr><th>$w < 0,30$</th><th>$0,30 \leq w \leq 0,45$</th><th>$0,45 < w$</th></tr><tr><td rowspan="2">Terminals</td><td>Width of plating defect (w_1)</td><td>$w_1 \leq 1/2 w$</td><td>$w_1 \leq 0,15$</td><td>$w_1 \leq 1/3 w$</td></tr><tr><td>Length of plating defect (l)</td><td colspan="3">$w_1 \leq w$</td></tr></table> <p>There shall be no defect of an area larger than 0,02 mm² for a terminal area of a large area such as a key contact</p>	Item		Finished line width, w			$w < 0,30$	$0,30 \leq w \leq 0,45$	$0,45 < w$	Terminals	Width of plating defect (w_1)	$w_1 \leq 1/2 w$	$w_1 \leq 0,15$	$w_1 \leq 1/3 w$	Length of plating defect (l)	$w_1 \leq w$			(1), (5), (6)
Item				Finished line width, w															
		$w < 0,30$	$0,30 \leq w \leq 0,45$	$0,45 < w$															
Terminals	Width of plating defect (w_1)	$w_1 \leq 1/2 w$	$w_1 \leq 0,15$	$w_1 \leq 1/3 w$															
	Length of plating defect (l)	$w_1 \leq w$																	
3	There shall be no defect such as poor contact and pit (hole or dent) that can be detected using a magnifying glass of 3× to 10× in the area of direct contact	(1), (4), (5)																	
X	The limit of a defect shall be agreed upon between user and supplier for special requirements	—																	

7.5.3.1.2 Solder plating (solder paste or dip solder plating including use of lead free solder)

The width of a plating defect at the terminal area, as shown in Figure 13(1), shall be no larger than one-half of the finished conductor width, and the length shall not exceed the width of the conductor.

Plating defects on land area, as shown in Figures 13(2) and (3), shall be less than 10 % of the total plated area (excluding the skipped plating area caused by adhesive squeeze-out).

Plating defects contacting the edge of a component hole, as shown in Figure 13(3), shall be no larger than one-third of the circumference. The area of a plating defect shall be covered with adhesive.

7.5.3.2 Penetration of plated metal or solder plating (Solder paste or dip solder plating including the use of lead free solder)

Penetration of plated metal or solder plating, as illustrated in Figure 14, shall meet the following requirements.

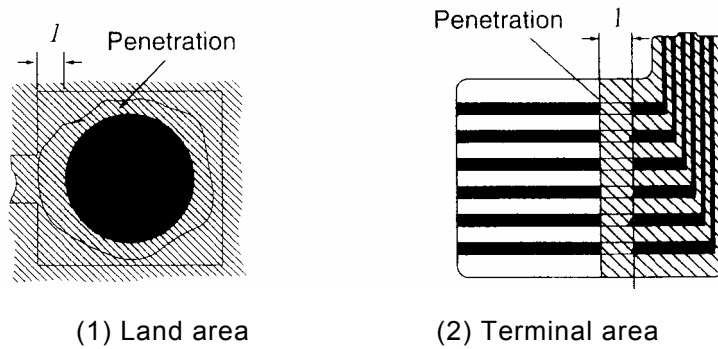


Figure 14 – Penetration of plated metal or solder

- a) The penetrated portion (l) between conductor and coverlay (covercoat and photosensitive resist) shall meet the requirement given in Table 12, as illustrated in Figure 14.

Table 12 – Requirement for metal penetration between conductor and coverlay

Unit: mm

Level	Requirement for metal penetration, l
1	$l \leq 0,5$
2	$l \leq 0,3$
3	$l \leq 0,1$

- b) The penetrated portion between the conductor and the base film shall meet the requirement given in Table 13.

Table 13 – Requirements for metal penetration between conductor and base film

Level	Requirement for metal penetration
1	Shall meet the requirement of 7.5.1.6
2 and 3	There shall be no visible penetration

7.5.3.3 Surface condition of plated metal and solder plating

7.5.3.3.1 Gold plating

Gold plating shall meet the requirement given in Table 14.

Table 14 – Gold plating

Level	Gold plating
1 and 2	Defect, such as stain, haze, and dirt which can be easily detected by the naked eye without the use of a magnification glass should be judged on the basis of a limit sample
3	There shall be no defect, such as stain, haze, discoloration, and dirt, detectable by observation with a magnification of 10×
X	The special requirement for any specific application shall be agreed upon between user and supplier

7.5.3.3.2 Solder plating (solder paste or dip solder plating including use of lead-free solder)

There shall be no darkened appearance (blackening discoloration).

7.5.3.3.3 Void in plated through hole

The number of plating voids illustrated in Figure 15 shall be no more than three per hole. The total area of voids for the entire hole wall (S_{sum}) for the total inner wall area of a hole (S_{total}) shall meet the requirement given in Table 15.

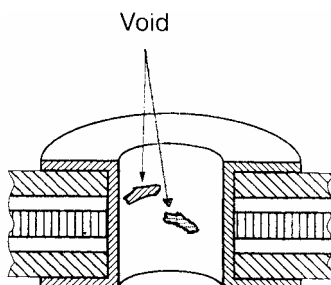


Figure 15 – Plating voids in plated-through hole

Table 15 – Allowable plating voids

Level	Total void area, S_{sum}
1 and 2	$S_{\text{sum}} < 1/3 S_{\text{total}}$
3	$S_{\text{sum}} < 10 S_{\text{total}}$

7.5.4 Visual inspection of edges of outline and holes

7.5.4.1 Tear and nick

There shall be no tear and nick except for slight cuts formed at the joining of blades which are allowed provided they are not visible without magnification, as illustrated in Figure 16.

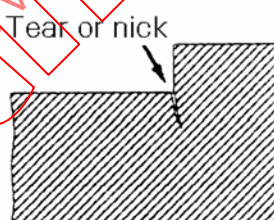


Figure 16 – Tear and nick

7.5.4.2 Burr

The height (h) of burr, as illustrated in Figure 17, shall be no larger than 0,1 mm.

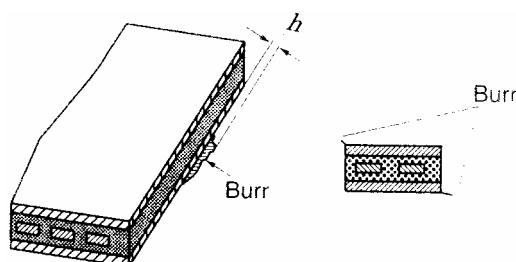


Figure 17 – Burrs

7.5.4.3 Thready burr

Two types of non-conductive thready burrs are illustrated in Figure 18. The length of thready burr at the outline edge (l_1 , l_2) shall be no longer than 1,0 mm. The length of burr at the hole edge (l_2) shall be no longer than 0,3 mm.

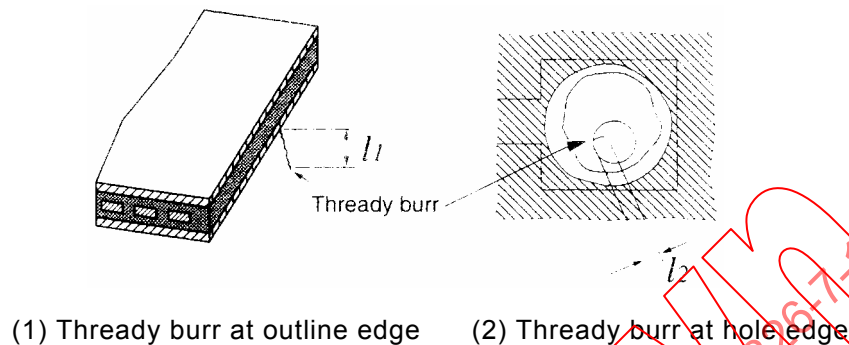


Figure 18 – Thready burrs

7.5.5 Visual imperfection related to stiffener bonding

7.5.5.1 Foreign substance between flexible printed board and stiffener

The bulge (t) of the FPC caused by a foreign substance sandwiched between the FPC and the stiffener, as illustrated in Figure 19, shall be no larger than 0,1 mm. The thickness of the stiffener shall also meet those specifications when the thickness of the printed board and stiffener are specified.

The size of the foreign substance shall be no larger than 5 % of the bonding area of the printed board and stiffener. There shall be no foreign substance in contact with the component hole or an outline edge of the board.

The length of a non-conductive thready foreign substance (l) protruding from the outline edge shall not exceed 1 mm.

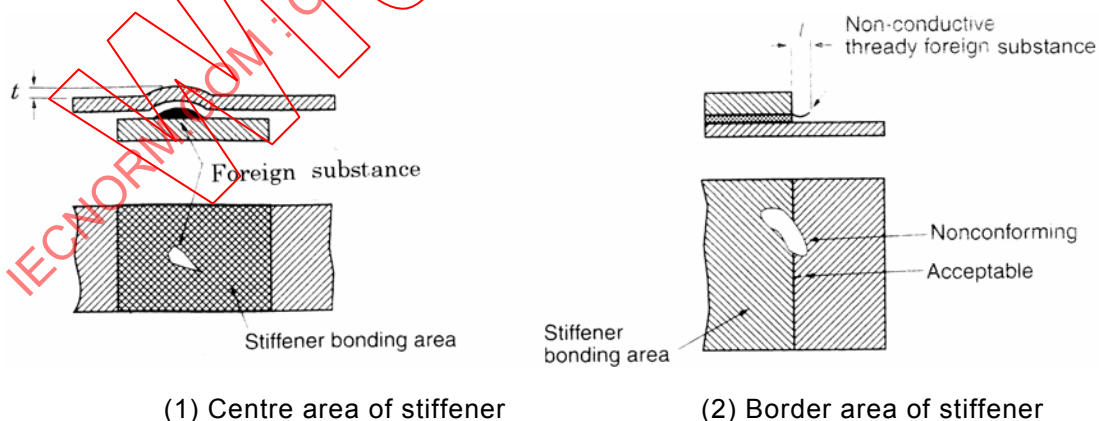


Figure 19 – Foreign substance between board and stiffener

7.5.5.2 Void between flexible printed board and stiffener

When the stiffener is bonded to FPC with thermosetting adhesive, the total area of voids, as illustrated in Figure 22, shall be no larger than 10 % of the total area of the stiffener. When other types of adhesive are used, the total area of voids shall be no larger than one-third of the stiffener area. There shall be no lifting and swelling at the tip for insertion to the connector.

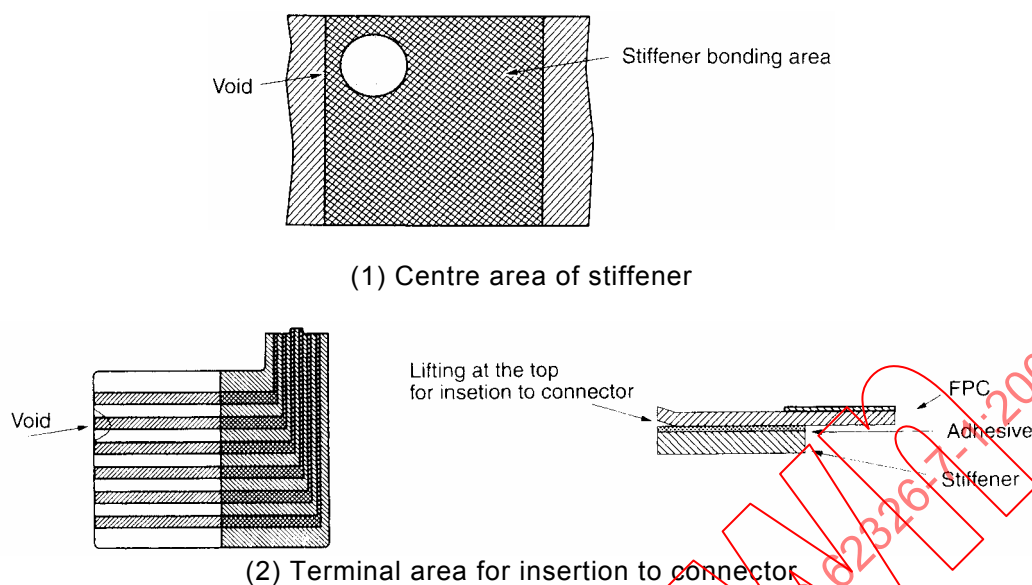


Figure 20 – Voids between board and stiffener

7.5.5.3 Defect of stiffener

7.5.5.3.1 Crack

Cracks, as illustrated in Figure 21, shall meet the requirement given in Table 16.

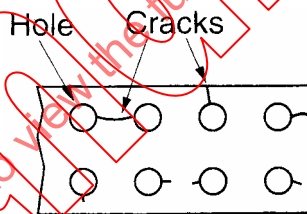


Figure 21 – Cracks

Table 16 – Cracks

Level	Cracks
1	There shall be no crack that could affect practical use
2 and 3	There shall be no crack that links two holes on the stiffener as well as a hole and the outline edge

7.5.5.3.2 Chip-off

The length (l) of a chip-off of stiffener, as illustrated in Figure 22, shall be no larger than 1 mm.

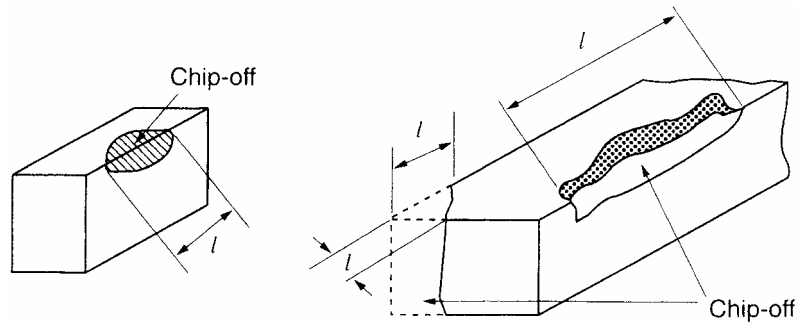


Figure 22 – Chip-off

7.5.5.3.3 Scratch

The allowable scratch shall be agreed upon between user and supplier if necessary.

7.5.5.3.4 Bow and twist

Bow and twist causing no problem in board assembly and instalment are acceptable.

7.5.6 Other visual inspection

7.5.6.1 Fixed substance on surface (excluding the area of exposed conductor)

7.5.6.1.1 Thermosetting adhesive

Thermosetting adhesive on the surface shall meet the requirement given in Table 17.

Table 17 – Thermosetting adhesive on surface

Level	Thermosetting adhesive on the surface
1 and 2	Cured adhesive, chip of overlay, covercoat or fibre stuck with adhesive hardly adhered on the surface is acceptable, provided they do not fall off when rubbed with an applicator impregnated with isopropyl alcohol. The thickness including the adhesive on surface shall meet the requirement where total thickness is specified
3	There shall be no visible substance stuck to the adhesive on the surface

7.5.6.1.2 Flux residues

Flux residue on the surface shall meet the requirement given in Table 18.

Table 18 – Flux residue on surface

Level	Thermosetting adhesive on the surface
1 and 2	When the surface is rubbed with an applicator impregnated with isopropyl alcohol, the applicator shall not be stained with flux residue
3	There shall be no visible flux residue on surface

7.5.6.1.3 Residue of metal powder (solder, aluminum, copper, etc.)

The following requirement shall apply only when the metal powder falling off the board does not cause any problem in the performance of equipment mounted with the flexible printed

circuit of the interest. The residue of the metal powder shall meet the requirement given in Table 19.

Table 19 – Residue of metal powder (solder, aluminum, copper, etc.)

Level	Residue of metal powder (solder, aluminum, copper, etc.)
1	The acceptable size and the number of metal grains shall be as follows: – for the grain diameter of 0,1 mm or larger and smaller than 0,03mm: 3 or less per product; – for the grain diameter of 0,05 mm or larger and smaller than 0,1mm: 10 or less per product
2	There shall be no visible metal powder residue
3	There shall be no metal powder residue detectable with a magnification 10×

7.5.6.1.4 Residue of adhesive

The residue of the adhesive shall meet the requirement given in Table 20.

Table 20 – Residue of adhesive

Level	Residue of adhesive
1 and 2	The acceptable size and the number of adhesive residue shall be as follows: – for the diameter of 1,0 mm or larger and smaller than 2,0 mm: 1 or less per product; – for the diameter of 0,1 mm or larger and smaller than 1,0 mm: 5 or less per product
2	There shall be no visible adhesive residue

7.5.6.2 Protrusion and dent

Wrinkle, uneven and crease which influence the characteristics on use and on the assembly process of a flexible print board are not permitted, even if there is no problem at the time of mounting and at use. A limit sample for these defects should be prepared if necessary. Examples of protrusions and dents are illustrated in Figure 23.

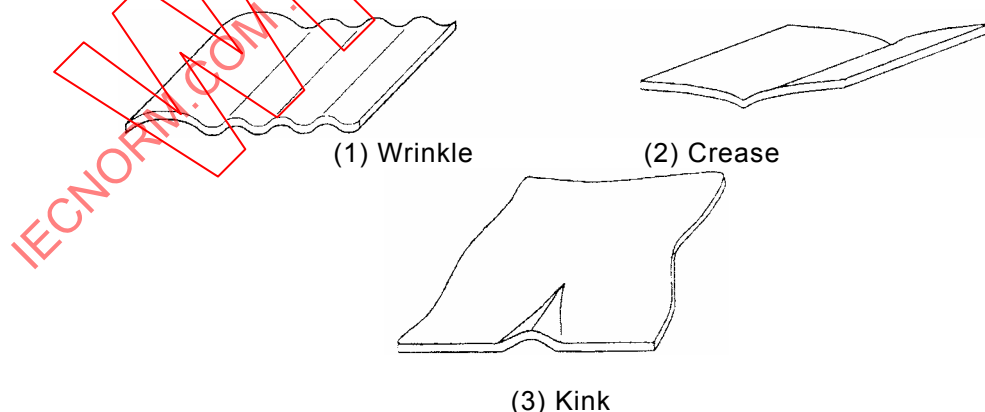


Figure 23 –Protrusion and dent on flexible printed board

7.5.6.3 Bow and twist

Bow, twist and the like, as illustrated in Figure 24, which may influence the characteristics on use and on the assembly process of a flexible print board are permitted if there is no problem at the time of mounting and at use in the field.

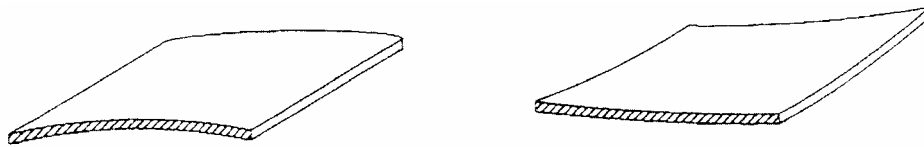


Figure 24 – Bow and twist

7.5.6.4 Conductor

Dent: Dent on a conductor, as illustrated in Figure 25, shall meet the requirement given in Table 21. Dent condition is usually difficult to judge (i.e., shape, size, and depth); accordingly, details should be agreed upon between user and supplier with reference to a limit sample prepared for evaluation.

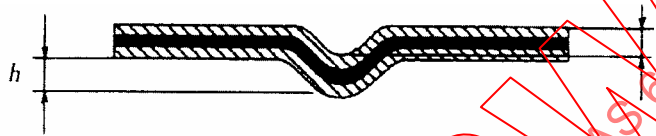


Figure 25 – Dent

Table 21 – Dent

Level	Depth of a dent, d
1 and 2	Depth (d) of a dent from the surface shall be $\leq 0,1$ mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
2	There shall be no dent visible from both sides

7.5.6.5 Base film side

a) Dent: Dent on the base film, as illustrated in Figure 25, shall meet the requirement given in Table 22.

Table 22 – Dent

Level	Dent
1 and 2	Depth (d) of a dent from the surface shall be no larger than 0,1 mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
2	There shall be no dent visible from both sides

b) Scratch on base film: The depth (d) of a scratch on a base film relative to the film thickness (t), as illustrated in Figure 26, shall meet the requirement given in Table 23. There shall be no sharp pressed mark, cut, tear, or delaminated adhesive layer. These defects shall not damage the bending property of the repeatedly flexing part.

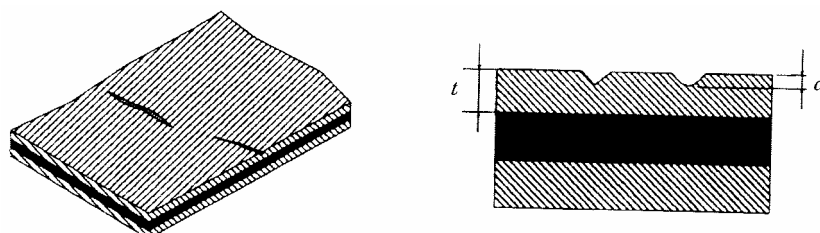


Figure 26 – Scratch on base film

Table 23 – Allowable scratches on base film

Level	Scratch on base film
1 and 2	$d \leq 1/3 t$
3	$d \leq 1/5 t$

7.5.6.6 Visual inspection of coverlay and covercoat

- a) Dent on coverlay and covercoat: Dents on coverlay and covercoat, as illustrated in Figure 25, shall meet the requirement given in Table 24.

Table 24 – Dents on coverlay and covercoat

Level	Depth of a dent, d
1 and 2	Depth (d) of a dent from the surface shall be no greater than 0,1 mm. When depth is difficult to measure, the height (h) of the back protrusion of the base film shall be regarded as equal to the depth (d) of a dent
3	There shall be no dent visible from both sides

- b) Scratch on coverlay and covercoat: The depth (d) of a scratch on the coverlay and covercoat relative to the thickness (t) of coverlay or covercoat, as illustrated in Figure 26, shall meet the requirement given in Table 25. There shall be no sharp pressed mark, cut, tear, or delaminated adhesive layer on the surface of coverlay or covercoat. These defects shall not damage the bending property of the repeatedly flexing portion.

Table 25 – Requirement for scratch on coverlay and covercoat

Level	Depth of a scratch, d
1	There shall be no exposure of conductor.
2	Depth (d) $\leq 1/3 t$
3	Depth (d) $\leq 1/5 t$

NOTE The thickness of the covercoat should be calculated by subtracting the thickness of the FPC without covercoat from the total FPC thickness.

7.5.6.7 Marking

Marking shall be legible.

8 Dimensional Inspections**8.1 Measurement of dimension**

Measuring methods for dimensions of the flexible printed board shall be in accordance with JIS C 5016, Clauses 3, 4 and 5 and 6.3.

8.2 External dimension

Measurement of external dimensions of the FPC shall meet the requirement given in Table 26.

Table 26 – Tolerance of external dimension

Level	Tolerance of external dimension
1 and 2	Tolerance of the external dimension of product: – for product size smaller than 100 mm in length: $\pm 0,30$ mm; – for product size of 100 mm or larger: $\pm 0,3$ %
3	Requirement shall be agreed upon between user and supplier

8.3 Thickness

Thickness shall meet the requirements given in Table 27.

Table 27 – Thickness tolerance

Level	Thickness tolerance
1 and 2	$\leq \pm 20$ % of the total thickness of the product
3	To be agreed upon between user and supplier

8.4 Hole diameter

Hole diameter shall meet the requirement given in Table 28.

Table 28 – Hole diameter and tolerance

Unit: mm

Thickness, t	Tolerance
$0,8 \leq t$	$\pm 0,20$
$0,2 < t < 0,8$	$\pm 0,10$
$t \leq 0,2$	$\pm 0,05$

8.5 Conductor width

Tolerances of the width of the finished conductor for designed conductor width shall meet the requirement given in Table 29.

Table 29 – Conductor width and tolerance

Unit: μm

Designed conductor width, w	Tolerance
$w < 50$	The requirement shall be agreed upon between user and supplier
$50 \leq w < 100$	± 25
$100 \leq w < 200$	± 50
$200 \leq w$	± 100

8.6 Cumulative pattern pitch

Table 30 gives the cumulative pitch as illustrated in the illustration.

Table 30 – Cumulative pattern pitch and tolerance

	Conductor pitch, P μm	Tolerance of the cumulative conductor pitch %
Level 1	$300 \leq P$	$\pm 0,3 \%$
Level 2	$150 \leq P < 300$	$\pm 0,2 \%$
Level 3	$100 \leq P < 150$	$\pm 0,15 \%$
Level X	$P < 100$	To be agreed upon between user and supplier

NOTE The length of each component is as follows. Connector: 11,4 mm, IC: 4,8 mm/side, and liquid crystal display: 35,6 mm.

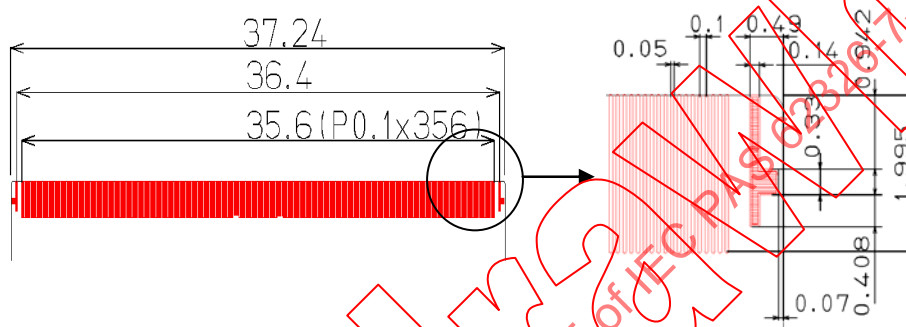


Figure a – ACF connector

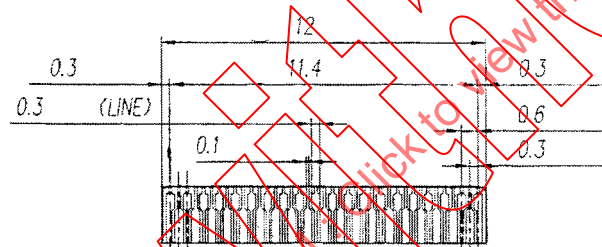


Figure b – Connector terminals

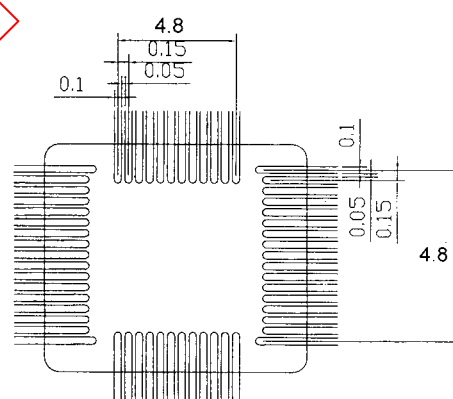


Figure c – COF terminals

Figure 27 – Cumulative pitch

8.7 Distance between hole centres

The distance between hole centres shall meet the requirements given in Table 31.

Table 31 – Tolerance of distance between hole centres

Level	Tolerance of distance between hole centers
1 and 2	For distance < 100 mm: $\pm 0,30$ 100 mm \leq for distances: $\leq 0,3 \%$ of the distance between hole centres
3	The requirements shall be agreed upon between user and supplier

8.8 Design minimum distance between board edge and conductor

Design minimum distance between a board edge and a conductor shall meet the requirement given in Table 32.

Table 32 – Design minimum distance between board edge and conductor

Level	Minimum distance between board edge and conductor
1 and 2	Design minimum distance between the board edge and the conductor shall not be $\leq 0,5$ mm
3	The requirements shall be agreed upon between user and supplier

8.9 Position accuracy

8.9.1 Position accuracy of holes

Position tolerance of a finished hole to the design position data shall be no larger than $\pm 0,3$ mm for an external dimension of less than 100 mm, and shall be no larger than $\pm 0,3$ % for an external dimension of over 100 mm, but except via holes.

8.9.2 Registration of hole to land

The minimum registration accuracy of a solderable finished land width (w), as illustrated in Figure 28, shall comply with the requirement given in Table 10.

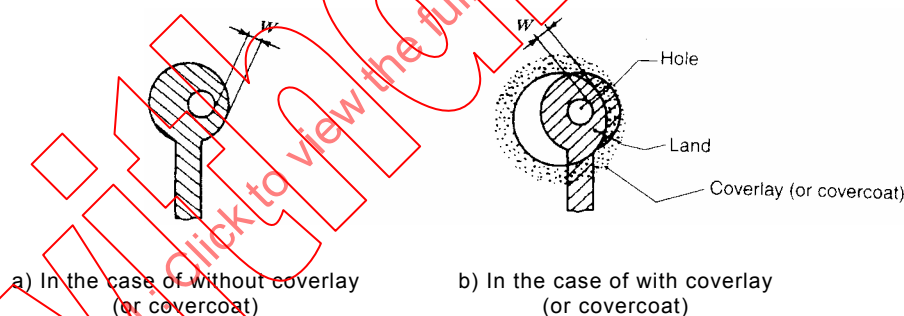


Figure 28 – Misregistration of hole and land

8.9.3 Registration of coverlay (or covercoat) to a land

The effective land area (S), as illustrated in Figure 29, shall comply with the requirement given in Table 10.

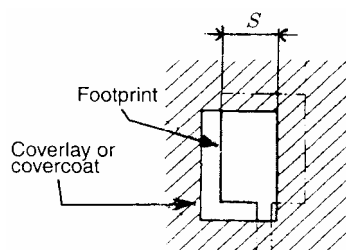


Figure 29 – Misregistration of land and coverlay (or covercoat)

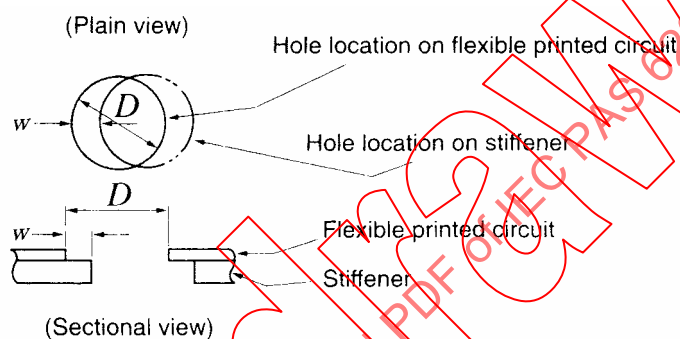
Table 33 – Effective land area

Level	Effective land area, S
1 and 2	Larger than 50 % of the designed land area
3	To be agreed upon between user and supplier

8.9.4 Registration accuracy of stiffener to FPC

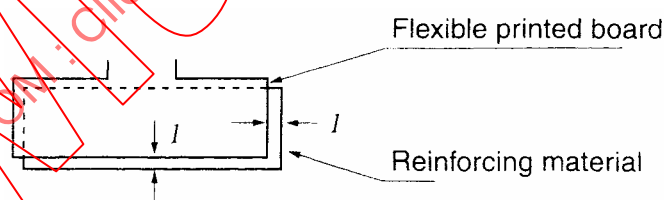
8.9.4.1 Hole registration

The deviation (w) between holes of the stiffener and the flexible printed circuit, as illustrated in Figure 30, shall be such that the difference ($D-w$) between the hole diameter (D) and the displacement (w) shall meet the tolerance requirement for the hole diameter (D).

**Figure 30 – Registration of holes**

8.9.4.2 Displacement of the outer dimensions

The displacement (l) between outer dimensions shall meet the requirements given in Table 34, as illustrated in Figure 31.

**Figure 31 – The displacement of the outer dimensions****Table 34 – Allowable displacement between outlines of the stiffener and the FPC**

Unit: mm

Level	Tolerance
1	$/ \leq \pm 0,5$
2	$/ \leq \pm 0,3$
3	$/ \leq \pm 0,2$

8.9.5 Registration of punched outline to conductor pattern

The registration of punched outline to conductor pattern shall meet the requirement given in Table 35.

Table 35 – Registration of punched outline to conductor patterns

Level	Requirement for registration
1 and 2	The edges of the outline of the board shall not be in contact with conductors, except for plating lead(s), isolated land(s), and conductor(s) for mechanical reinforcement
3	The clearance between the outline edge and the conductor shall be no smaller than 0,1 mm, except for plating lead(s), isolated land(s) and conductor(s) for mechanical reinforcement

8.10 Registration of pressure sensitive or heat activated adhesive (including adhesive squeeze-out) to flexible printed board and stiffener

The displacement (l) of pressure-sensitive or heat-activated adhesives from the FPC and stiffener (including adhesive squeeze-out), as illustrated in Figure 32, shall be $\pm 0,5$ mm. The registration of the adhesive at component holes shall meet the requirement for the tolerance of the hole diameter.

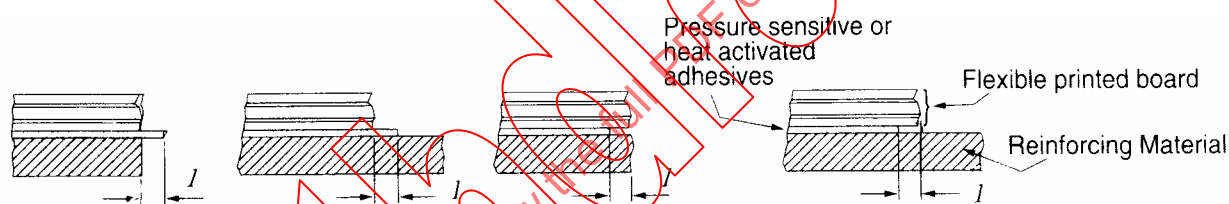


Figure 32 – Registration of pressure-sensitive or heat-activated adhesive from flexible printed board and stiffener (Including adhesive squeeze-out)

8.10.1 Plating thickness of copper plated-through holes

The thickness of the plated copper of the plated-through holes shall be 0,004 mm min.

9 Electrical performance test

The electrical performance of the FPC shall be tested in accordance with JIS C 5016. The test items and requirements are given in Table 36.

Table 36 – Electrical properties of flexible printed boards

Item No.	Item		Requirement	Test method (JIS C 5016)
9.1	Conductor resistance		Shall be agreed upon between user and supplier	7.1 (Conductor resistance)
9.2	Insulation resistance of surface layers	As received	$5 \times 10^8 \Omega \leq$	According to 7.6 (Insulation resistance of surface layers)
		After humidity test	Level 1: shall retain the electrical functions. Level 2: $1 \times 10^8 \Omega \leq$ Level 3: $5 \times 10^8 \Omega \leq$	9.4 (Temperature and humidity cycling test) and according to 7.6
9.3	Dielectric withstanding voltage of surface layers		There shall be no flashover when 500 V a.c. is applied.	7.5 (Dielectric withstanding voltage, surface layers)
9.4	Open circuit of the conductor		1 k Ω *	7.7-2 (Circuit continuity test)
9.5	Short circuit between conductors		$\leq 100 \text{ k}\Omega$ *	7.7.1 (Circuit isolation test)
* The criteria values for open circuit and short circuit for judging the product performance may not necessarily be these values.				

10 Mechanical performance test

The mechanical performance of FPCs shall be tested in accordance with JIS C 5016. The test items and specifications are given in Table 37.

Table 37 – Mechanical properties of flexible printed boards

Item No.	Item	Property requirements	Test method (JIS C 5016)
10.1	Peel strength	Conductor	0,49 N/mm \leq
		Coverlay	0,34 N/mm \leq
		Stiffener	Thermosetting adhesives: 0,34 N/mm Pressure sensitive adhesives: 0,15 N/mm \leq
10.2	Pull-out strength for plain hole and footprint	Level 1: Not specified Levels 2 and 3: 1 N/mm ² \leq	8.2 (Pull-out strength for plain holes) and 8.3 (Pull-out strength for footprints)
10.3	Plating adhesion	There shall be no peel-off	8.4 (Plating adhesion)
10.4	Solderability	The well-wetted area shall be more than 95 % of the total plated area. This does not apply to FPCs with polyester base film	10.4 (Solderability)
10.5	Flexural endurance	FPCs with coverlay shall satisfy the specified bending radius and the bending frequency based on the repetition speed, which are agreed between user and supplier	8.6 (Flexural endurance) The rate of 1 000 cycles/min or higher is preferred to save the testing time
10.6	Bending resistance	FPCs with coverlay shall satisfy the specified bending curvature radius and the loaded bending frequency which are agreed between user and supplier	8.7 (Bending resistance)

11 Environmental performance

The environmental test of FPCs shall be made in accordance with JIS C 5016. The test items and requirements are given in Table 38.

Table 38 – Environmental tests and requirements

Item No.	Item		Requirement	Test method JIS C 5016
11.1	Temperature cycling		Shall meet the requirements before and after the test for the items and conditions agreed upon between user and supplier	9.1 (Temperature cycling)
11.2	Humidity test	Stationary condition	Same as 11.1	9.5 (Humidity test, stationary condition)
		Temperature/humidity cycling	Same as 11.1	9.4 (Humidity test, temperature/humidity cycling)
11.3	Thermal shock	High temperature dipping	Same as 11.1	9.3 (Thermal shock, low temperature/high temperature cycling)
		Low temperature/high temperature cycling	Same as 11.1	9.2 (Thermal shock, low temperature/high temperature cycling)
11.4	Thermal shock resistance of connection between layers (copper plated-through hole, etc.)		The variation in connection resistance between layers (copper plated-through hole, etc.) shall be less than 20 %	10.2 (Thermal shock resistance of copper plated-through holes)
11.5	Migration		$10^{-8} \Omega \leq$	Annex B of this document
11.6	Whisker		To be agreed upon between user and supplier	Annex C of this document

12 Chemical resistance

There shall be no swell or delamination when tested in accordance with JIS C 5016, 10.5. There shall be no appreciable damage of symbol marks.

13 Cleanliness

The measuring method and the requirement shall be agreed upon between user and supplier.

14 Flame resistance

The flame resistance shall be agreed upon between user and supplier.

15 Marking, packaging, and storage

These items should normally be agreed upon between user and supplier. The items in 15.1 and 15.2 are given just as guidelines.

15.1 Marking on products

- a) Product name or product's code name
- b) Name of manufacturer or the code name

15.2 Marking on package

- a) Product type (name or symbol expressing the FPC shall be marked where it is readily seen)
- b) Product name or its code name
- c) Number of products in the package
- d) Production lot number or year/month of manufacturing
- e) Name of manufacturer or its code name

15.3 Packaging and storage

15.3.1 Packaging

Packaging shall meet the requirements given in Table 39.

Table 39 Requirements for packaging

Level	Requirement
1	The product shall be packaged so that it is not damaged during transportation
2	In addition to the requirement for level 1, humidity shall be controlled during storage at room temperature
3	In addition to the requirement for levels 1 and 2, any requirement agreed upon by user and supplier shall be incorporated

15.3.2 Storage

FPCs shall be stored in a storage that is equipped with suitable humidity control.

15.3.3 Handling

Annex A gives the recommendation for preventing accidents caused by the handling of FPCs by customer.

Annex A

Handling instruction manual handling of polyimide-base FPC

A.1 Storage and handling

Wipe off moisture and/or chemical substance(s) attached to the product surface during storage and/or handling. These substances may cause discoloration and/or deterioration of the product.

The tarnish protection coating on the conductor is valid for approximately six months after production in a storage where temperature and humidity are controlled, whereas the plated and cream-solder-coated surface is valid for approximately one year.

In addition to the precautions to prevent mechanical damage to the boards caused by careless handling or stacking of boards, it is very important to protect boards against contamination by foreign substances. Oil component may be transferred from human skin to a board causing contamination, stain or discoloration when the board is handled for test or installation to an automatic processing machine. Hand cream containing silicone can cause poor adhesion of photoresist and coverlay layers.

Protection gloves shall be used to prevent contamination.

Periodical change of gloves should be observed. Generation of minute fibre dust from the gloves should be checked.

A.2 Component mounting and installation to equipment

Torque to tighten screws and caulk metal plates shall be appropriately adjusted. Too high a torque may break materials.

A.3 Soldering

A.3.1 Pre-treatment

Polyimide used as a base film of FPCs and as a coverlay absorbs moisture easily (i.e., the simple film will be saturated with water vapour in approximately 4 h if a polyimide film is left in the open air). This may readily cause blistering of the FPC by a rapid temperature change when soldering is carried out using a reflow furnace or flow soldering equipment. Pre-drying of the FPC to remove absorbed moisture should be added as a pre-treatment process before the assembly process.

Depending on the composition of the FPC, the following pre-drying conditions are recommended as given in Table A.1.